

Title	Page	Title	Page	Title	Page
COVER PAGE	1	(RSVD)	41	(RSVD)	81
BLACK DIAGRAM	2	(RSVD)	42	(RSVD)	82
CPU_DISPLAY	3	DC IN CONN	43	(RSVD)	83
CPU_DDR_CHA	4	(RSVD)	44	(RSVD)	84
CPU_DDR_CHB	5	RT6575D_5V_S5/3D3V_S5	45	(RSVD)	85
CPU_LPSS/ISH_I2C	6	NCP81206MN_CPU_VCORE(1/3)	46	(RSVD)	86
CPU_POWER1	7	NCP81206MN_CPU_VCORE(2/3)	47	(RSVD)	87
CPU_POWER2	8	NCP81206MN_CPU_VCORE(3/3)	48	DUMMY PARTS	88
PCH_POWER1	9	(RSVD)	49	SCREW HOLE/EMI CAP	89
CPU_POWER CAP1	10	NCP81253MN_IV_VCCSA	50	(RSVD)	90
CPU_POWER CAP2	11	VDDQ/VT/2D5V_S3	51	(RSVD)	91
DDR4-SODIMM1	12	ID0V_S5/IV_VCCST/IV_VCCIO	52	(RSVD)	92
DDR4-SODIMM2	13	G9661_ID8V_S5	53	(RSVD)	93
CPU_STRAP	14	(RSVD)	54	(RSVD)	94
CPU_PCIE/SATA/USB3/USB2	15	LCD CONN	55	(RSVD)	95
CPU_CLOCK	16	(RSVD)	56	(RSVD)	96
CPU_AUDIO/SDIO/SDXC	17	HDMI LEVEL SHIFTER/CONN	57	(RSVD)	97
CPU_LPC/SPI/SMBUS/CLINK	18	RTD2136 eDP to LVDS	58	CLOCK	98
CPU_CS-2/EMMC	19		59	XDP	99
CPU_POWER MANAGEMENT	20	HDD	60	TABLE OF CONTENT	100
CPU_VSS	21	WLAN	61	CHANGE HISTORY	101
CPU_JTAG/MISC	22	(RSVD)	62	POWER SEQUENCING	102
CPU_RSVD/CFG	23	SSD_KEY.M	63	POWER BLOCK DIAGRAM	103
SIO_IT8732F	24	PWR BTN/SIDE KEY/LED	64	SMBUS BLOCK DIAGRAM	104
SPI/RTC	25	(RSVD)	65	THERMAL/AUDIO BLOCK DIAGRAM	105
(RSVD)	26	(RSVD)	66		
AUDIO_ALC255	27	(RSVD)	67		
CAMERA CONN	28	DEBUG HEADER	68		
Audio Jack/SPK CONN	29	(RSVD)	69		
(RSVD)	30	(RSVD)	70		
LAN_RTL8111H	31	(RSVD)	71		
RJ45+TRANSFORMER	32	(RSVD)	72		
SD/CR_RTSS176	33	(RSVD)	73		
USB2 CONN	34	(RSVD)	74		
USB3 CONN	35	(RSVD)	75		
(RSVD)	36	(RSVD)	76		
(RSVD)	37	(RSVD)	77		
(RSVD)	38	(RSVD)	78		
(RSVD)	39	(RSVD)	79		
POWER SEQUENCING	40	(RSVD)	80		

Eiffel238i-2 Schematics Document

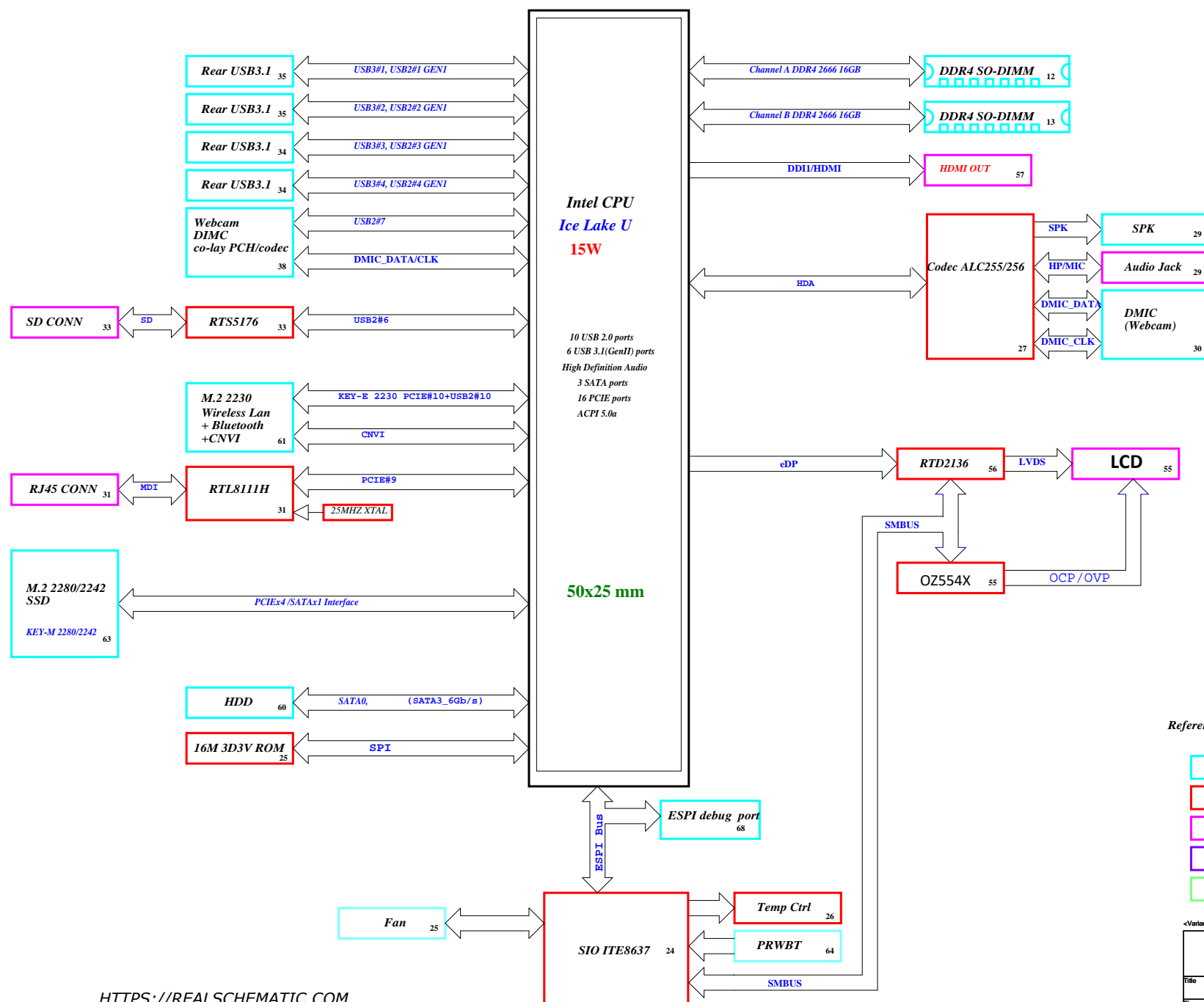
BOM Configuration
(R_):Unmount
(O_):OCP
(DBG_):Debug

Project code :
PCB No :19450
Revision :SA
Project Name :EIFFEL238i-2
Size :264.0mm x 105.3mm

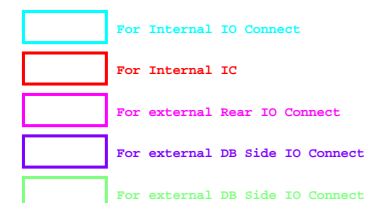
Eiffel238i-2_ICL Block Diagram

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Signal



Reference Design CPU:
I/O:Eiffel238i-KBLR



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: C Document Number: **Eiffel-2 ICL U** Rev: SA

Date: Friday, December 27, 2019 Sheet: 2 of 106

Main Func = CPU

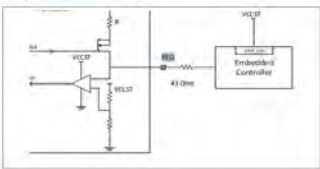
5.5.4 CATERR# Topology

CATERPILLAR's reliability system has experienced a catastrophic error and cannot continue to operate. The full Lake groupware will not allow for non-reversible machine check errors and other software error conditions to occur. CATERPILLAR is an AppleLink/Apple II system that is not designed with an active backchannel (OOP). This system can be converted to a LEO if needed. Also, this system should have an external hard disk for data during system.

Figure 5-48. Routing Illustration for CATERPILLAR Topology

Table 5-105. **LAVERNE** Routing Guidelines (Sheet 5 of 5)[illegible]

Figure 2-2. Example for PEC1 EC Connection



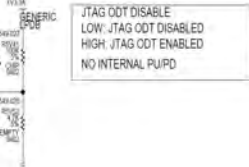
FOLLOW CRB BY HOWARD
20191002

Table 3-3. Debug Port Signal Mapping

[illegible]

FOLLOW CRB BY HOWARD
20191002

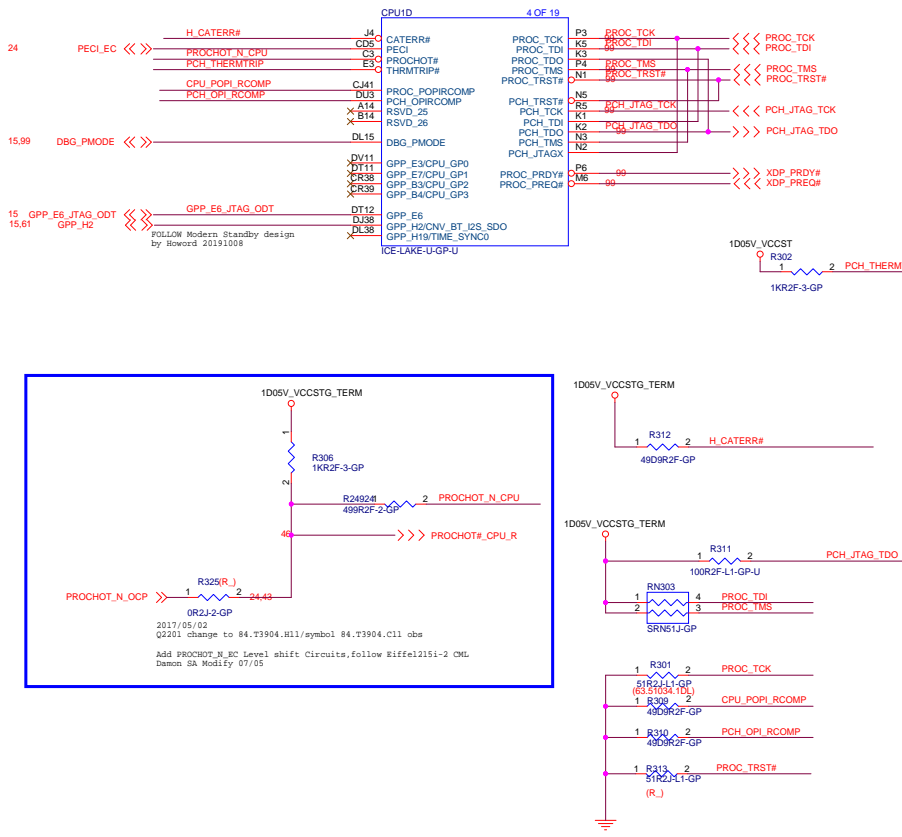
PLACE RA AND FB CLOSE TO THE SPI SIGNAL TO AVOID STIR



MAF/SAF STRAP
LOW-> MAF ENABLE
HIGH-> SAF ENABLE
WEAK INTERNAL PD 20K

+V3.3A
 GENERIC
 LP08
 1-X
 JRC2
 HDR 1X2
 2
 SAF_ENABLE
 JRC35
 2.2K

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Date 13-1, Primary Design Port - Dual Scan Chain Only Routing Guidelines (Sheet 1 of 3)	
Rev. / Comment	Revision Number

[illegible]

Table 13-1. Primary Debug Port – Dual Scan Chain Only Routing Guidelines (Sheet 2 of 3)

[illegible]

Table 13-1. Primary Debug Port - Dual Scan Chain Only Routing Guidelines (Sheet 3 of 3)

Port/Signal	Routing Rules
UTL_TSD	<ul style="list-style-type: none"> *Route from UTL_TSD to bus Lane PROG_TSD and PROG_TSD_TSL. *Make sure not to route the traces no more than 20mm from UTL_TSD pin. • Test Pad Placement: <ul style="list-style-type: none"> • Must placed on secondary side • Place to within 30mm of bus lane and within 20mm of termination. • Pad size: Minimum 0.452mm, preferred pad size 0.813mm • Refer to section 13.1.4 for additional design requirements to support Intel® Silicon • Length: Minimum 100 above 50% pad length to WCCSG or equivalent *Send to within 20mm of PROG_TSD_TSL pin (either PROG_TSD pin or the termination). <p>Trace length: 20mm</p> <ul style="list-style-type: none"> *The stub length should be minimized whenever possible <p>Trace-to-Trace spacing: No limit. At least 1 trace width when possible</p> <p>Maximums: None</p> <p>Maximum Trace Length: 150mm [For each segment, measured from Delag Port to bus Lane pin]</p> <p>Length Matching: matching to ± 0.4 mils of TSD</p> <ul style="list-style-type: none"> • Match PROG_TSD to PROG_TSD_TSL • Match PROG_TSD to PROG_TSD_TSL net • Length matching is recommended but is not optional (Differential Length matching to TSD might also operating at higher TSD frequencies) <p>Refer to Section 13.1.4 for additional design port PCB layout rules.</p> <p>Refer to Section 13.1.6 for design port de-termination rule.</p>
UTL_TSD	<ul style="list-style-type: none"> *Route from UTL_TSD to bus Lane PROG_TSD and PROG_TSD_TSD. *Make sure not to route the traces no more than 20mm from UTL_TSD pin. • Test Pad Placement: <ul style="list-style-type: none"> • Must placed on secondary side • Place to within 30mm of bus lane and within 20mm of termination. • Pad size: Minimum 0.452mm, preferred pad size 0.813mm • Refer to section 13.1.4 for additional design requirements to support Intel® Silicon • Length: Minimum 100 above 50% pad length to WCCSG or equivalent *Send to within 20mm of each bus lane pin. <p>Trace length: 20mm</p> <ul style="list-style-type: none"> *The stub length should be minimized whenever possible <p>Trace-to-Trace spacing: No limit. At least 1 trace width when possible</p> <p>Maximums: None</p> <p>Maximum Trace Length: 150mm [For each segment, measured from Delag Port to bus Lane pin]</p> <p>Length Matching: matching to ± 0.4 mils of TSD</p> <ul style="list-style-type: none"> • Match PROG_TSD to PROG_TSD_TSL net • Match PROG_TSD to PROG_TSD_TSL net • Length matching is recommended but is not optional (Differential Length matching to TSD might also operating at higher TSD frequencies) <p>Refer to Section 13.1.4 for additional design port PCB layout rules.</p> <p>Refer to Section 13.1.6 for design port de-termination rule.</p>

13.1.1.2 Primary Debug Port: Observation Ports (CFG[0:19]) and PREQ#/PBDY pins Routing Guidelines

The library contains the following 10 observation data signals (OBSDATA ports) and associated control signals. A control signal is shown.

Table 13-2. Primary Debug Port - Observation Pine Routing Guidelines (Sheet 1 of 2)

[illegible]

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU_DISPLAY			
Size	Document Number	Rev	
	Eiffel-2_ICL_U	S	
Date:	Friday, December 27, 2019	Sheet	3 of 106

Port	Function	DDI Signal Name	eDP* Signal Name
DDIA/B	Main Link	DDIX_TXP[0]	DDIX_eDP_LANE0_P
		DDIX_TXN[0]	DDIX_eDP_LANE0_N
		DDIX_TXP[1]	DDIX_eDP_LANE1_P
		DDIX_TXN[1]	DDIX_eDP_LANE1_N
		DDIX_TXP[2]	DDIX_eDP_LANE2_P
		DDIX_TXN[2]	DDIX_eDP_LANE2_N
		DDIX_TXP[3]	DDIX_eDP_LANE3_P
		DDIX_TXN[3]	DDIX_eDP_LANE3_N
	Aux	DDIX_AUX_P	DDIX_eDP_AUX_P
		DDIX_AUX_N	DDIX_eDP_AUX_N
		DISP_RCOMP	Pull Down to VSS via 150 ohm resistor
		DISP_UTILS	Recommended 50 Ω nominal trace impedance with reasonable noise solution Requires level shifting on the platform.
	HPD	DDISP_HPDA - DDIA	eDPA_HPDP
	VDD Enable	EDP_VDDEN - DDIA	eDPA_VDDEN
	BKLT Enable	EDP_BKLTEN - DDIA	eDPA_BKLT_EN
	BKLT Control	EDP_BKLTCTL - DDIA	eDPA_BRIGHTNESS

Note: x can be DDI port A or B

Note: x can be ODI port A or B

Table 1-6. HD04A's Channels			
Port	Port Name	DEF Internal Name	HD04P's Internal Name
DCH B	Main Link	DCHB_TSP0_P1	DCHB_HDMI_DATA2_P
		DCHB_TSP0_P2	DCHB_HDMI_DATA2_N
		DCHB_TSP0_P3	DCHB_HDMI_DATA3_P
		DCHB_TSP0_P4	DCHB_HDMI_DATA3_N
		DCHB_TSP0_P5	DCHB_HDMI_DATA4_P
		DCHB_TSP0_P6	DCHB_HDMI_DATA4_N
		DCHB_TSP0_P7	DCHB_HDMI_CIR_P
		DCHB_TSP0_P8	DCHB_HDMI_CIR_N
		DCHB_TSP0_P9	DCHB_HDMI_CIR_P
		DCHB_TSP0_P10	DCHB_HDMI_CIR_N
EDCH	Ed Channel	EDCH_CHANNELS	DCHB_HDMI_CIR_P
HD0		HD0B_CHANNELS	DCHB_HDMI_CIR_N
Type C *	Main Link	TC0P_TSP0_P0	DCHB_HDMI_DATA2_P
		TC0P_TSP0_P1	DCHB_HDMI_DATA2_N
		TC0P_TSP0_P2	DCHB_HDMI_DATA3_P
		TC0P_TSP0_P3	DCHB_HDMI_DATA3_N
		TC0P_TSP0_P4	DCHB_HDMI_DATA4_P
		TC0P_TSP0_P5	DCHB_HDMI_DATA4_N
		TC0P_TSP0_P6	DCHB_HDMI_CIR_P
		TC0P_TSP0_P7	DCHB_HDMI_CIR_N
		TC0P_TSP0_P8	DCHB_HDMI_CIR_P
		TC0P_TSP0_P9	DCHB_HDMI_CIR_N
EDCH	Ed Channel	EDCH_CHANNELS	DCHB_HDMI_CIR_P
HD0		HD0B_CHANNELS	DCHB_HDMI_CIR_N
HD1		HD1B_CHANNELS	DCHB_HDMI_CIR_P
HD2		HD2B_CHANNELS	DCHB_HDMI_CIR_N

Note: * can be used 1-4 dependent on the DCHB.

HD0 Connects to HD0B via a 400 ohm resistor.

FOLLOW CRB

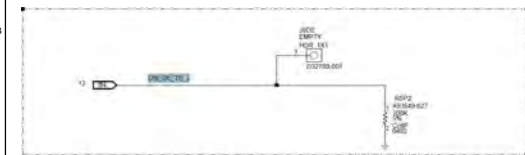


Table 5-28. DisplayPort® Signals

Description	Signal Mapping			Note
	Ice Lake Processor	Ice Lake PCH	CRB DisplayPort* Mapping	
Main Link (Tx)	DDIx_TXP[N][3:0]	N/A	N/A	1
	TCpTx_TX_P/N[1:0] and TCpTx_TXRX_P/N[1:0]	N/A	N/A	2
	DDIx_AUX0/N	N/A	N/A	1
Aux Channel	TCpTx_AUX_P/N	N/A	N/A	2
Hot Plug Detect	N/A	DDSP_HPD_x	N/A	
DISP_UTILS	Recommend 50 ohm nominal trace impedance. Requires level shifting on the platform.			
DISP_RCOMP	150 ohm +/-1% pull-down to VSS			3

Notes:

1. Signals names apply for DDI A/B ports.
2. Signal's names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm

Notes:

1. Signals names apply for DD1 A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm

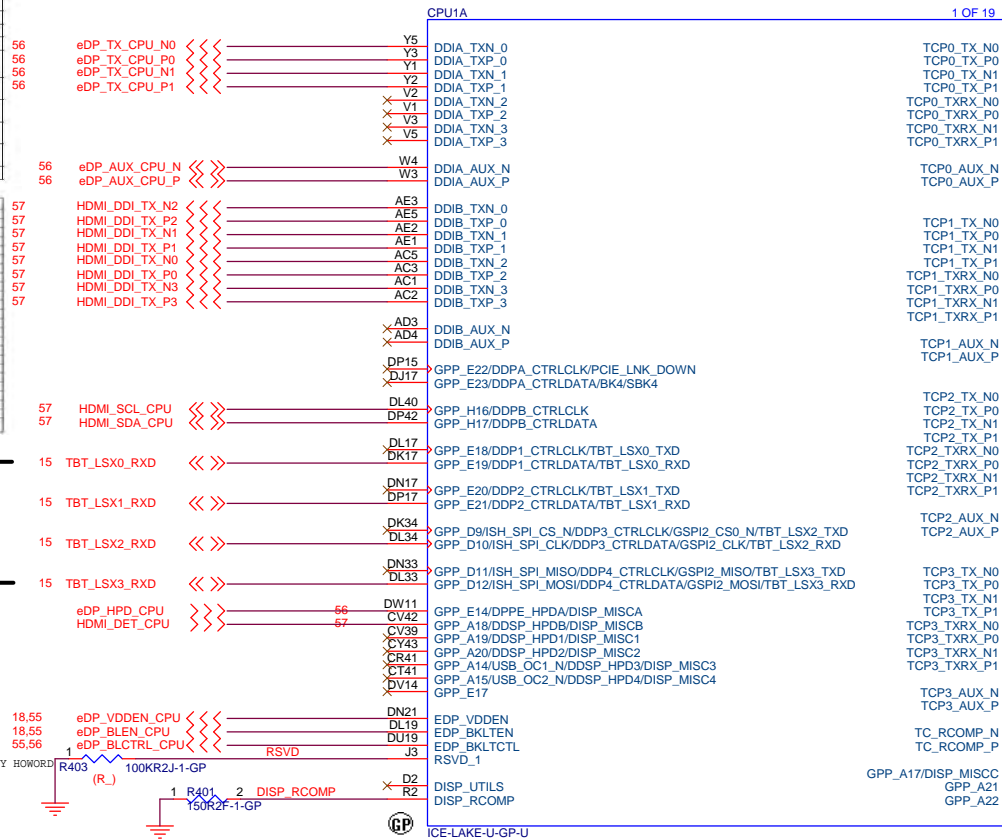


Table 1-3. Type-C Low speed and RCOMP Checklist

Function	Port	Pin Name	Schematic Notes
Low Speed Differential	Port 0	USB2N_1[1:10]	Can be any of the USB2 ports from the PCH 1:10.
		USB2P_1[1:10]	
	Port 1	USB2N_1[1:10]	
		USB2P_1[1:10]	
	Port 2	USB2N_1[1:10]	
		USB2P_1[1:10]	
	Port 3	USB2N_1[1:10]	
		USB2P_1[1:10]	
Resistor Compensation	All	TC_RCOMP_N	150Ω +/-1% between TC_RCOMP_N and TC_RCOMP_P. Provide good noise isolation. Platform Rdc < 0.5ohms for the sum of both signals.
		TC_RCOMP_P	

Note: Port 3 available on ICL-U only

Note: Port 3 available on ICL-U only

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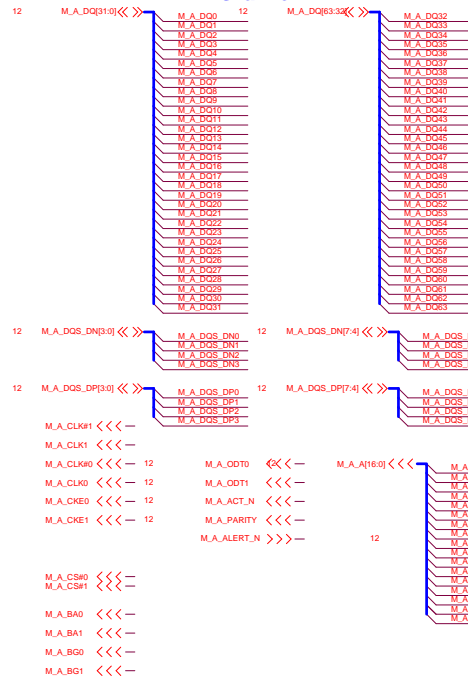
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (DDI/EDP/TBT/TPC/)
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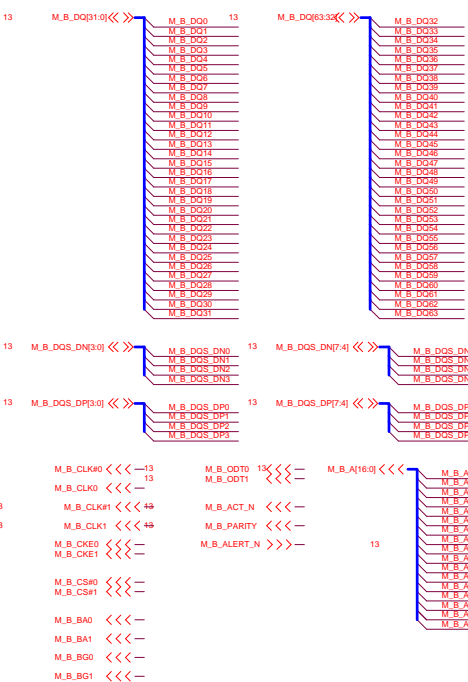
Size A3	Document Number Eiffel-2 ICI II	Rev SA
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Date: Friday, December 27, 2019 Sheet 4 of 106

Channel A



Channel B

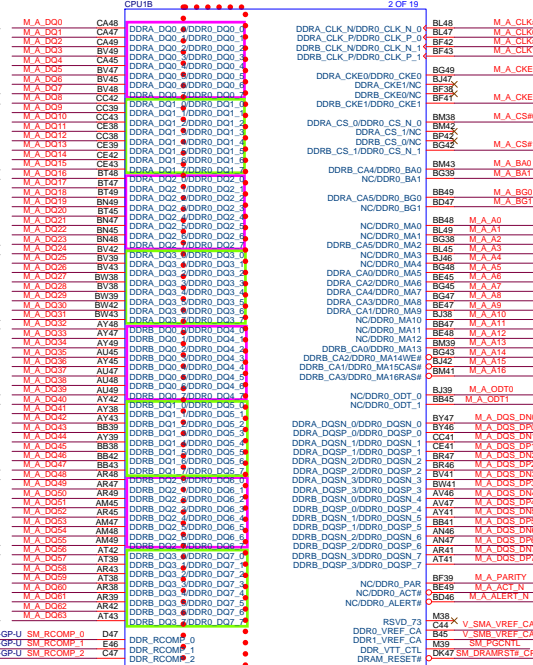


SSID = CPU

DDR4 ball type: non-interleave Type

Document Number: 572795 Ver 1.6

non-interleave



non-interleave



SDIMM follow CSB

SDIMM follow CSB

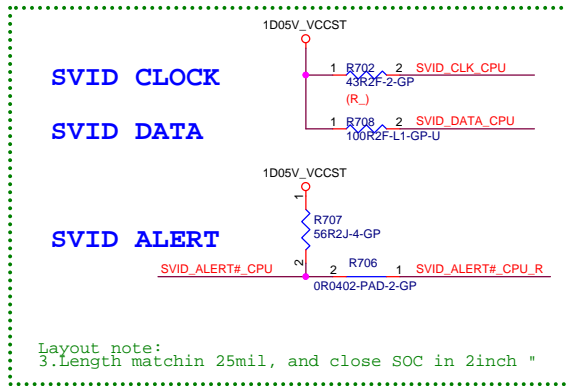
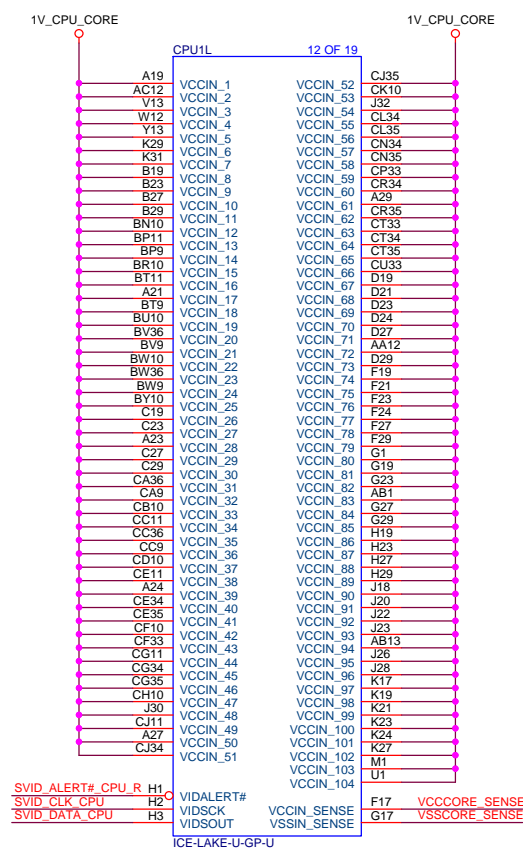
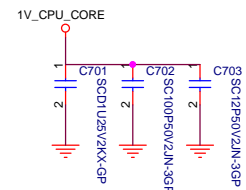
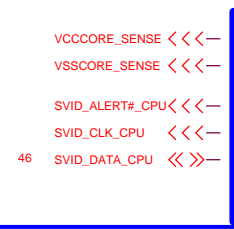
M_A_DQ80
M_A_DQ81
M_A_DQ82
M_A_DQ83
M_A_DQ84
M_A_DQ85
M_A_DQ86
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M_B_DQ80
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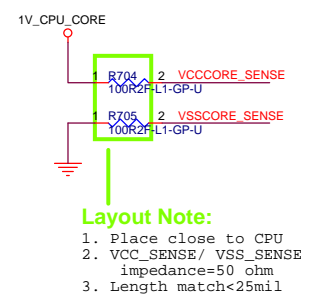
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CPU (DDR)			
File	Document Number	Rev	SA
Size	Effel2 ICL U		
Date	Friday, December 21, 2018	Sheet	5 of 108



Layout note:
3.Length matchin 25mil, and close SOC in 2inch "



Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

5.5.10 SVID Topology

Figure 5-54. Routing Illustration for SVID Topology

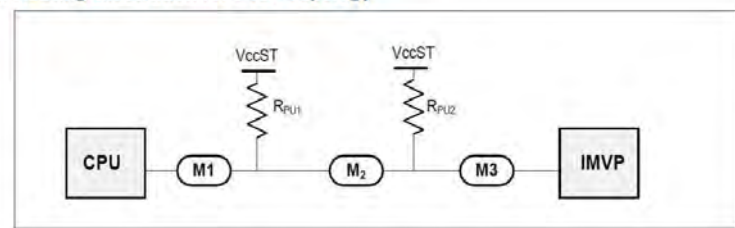
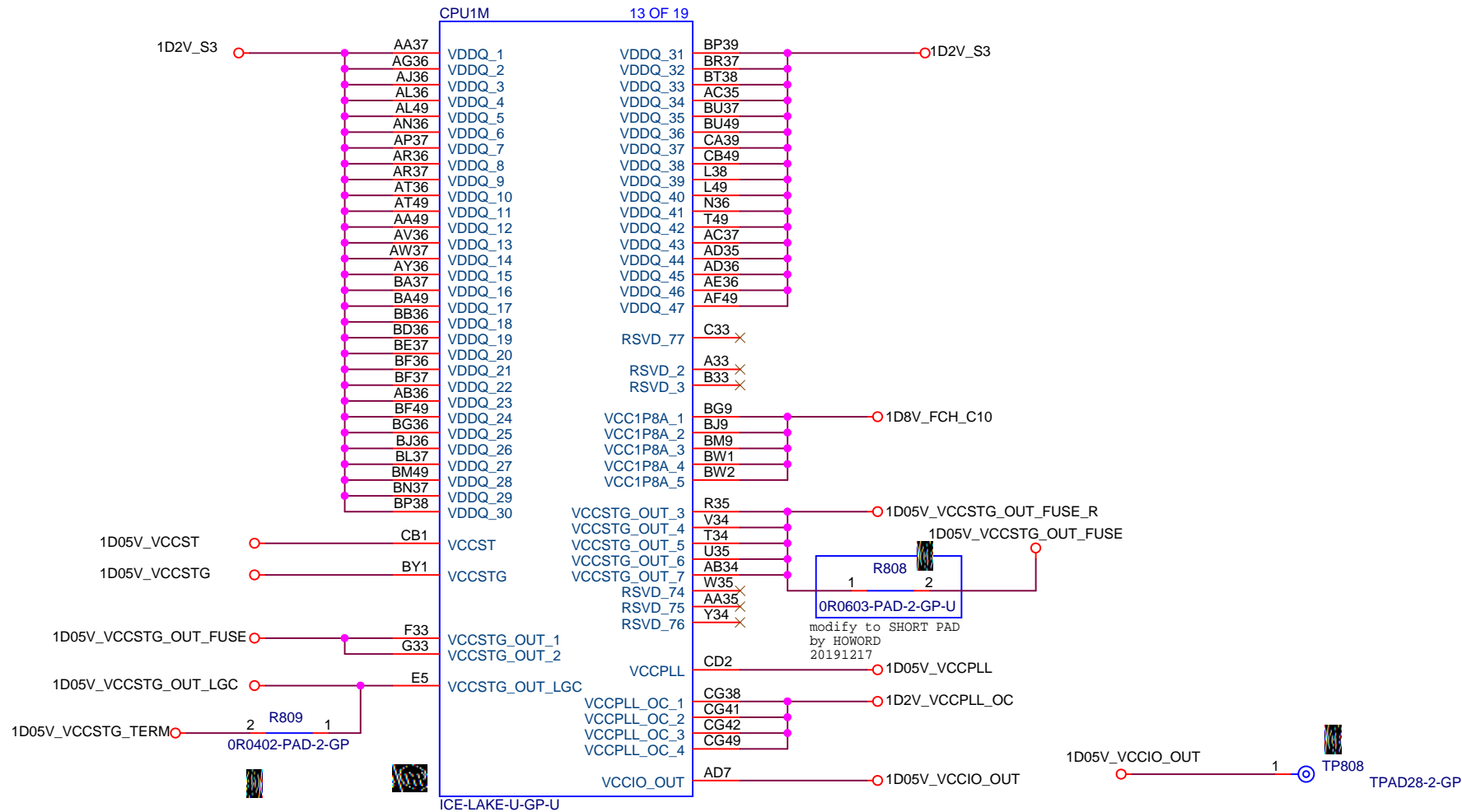


Figure above demonstrates Routing Illustration for SVID Topology, each trace from CPU to VR represents 3 signals: VIDSOUT, VIDSCK, VIDSALERT#.

Table 5-75. SVID Routing Guidelines

Segment	Tline Type	Reference	Via Count	Max Length, mm	
				Segment	Total
M1	MS/SL/DSL	VSS		75	530
M2	MS/SL/DSL	VSS		380	
M3	MS/SL/DSL	VSS		75	
Topology Guidelines					
SVID Signals		VIDSOUT, VIDSCK, VIDSALERT#			
VIDSOUT platform resistors		Rpu1=100Ω, Rpu2=100Ω			
VIDSCK platform resistors		Rpu1=Empty, Rpu2=45Ω			
VIDSALERT# platform resistors		Rpu1=56Ω, Rpu2=Empty			
Platform: Wistron Corporation					
Route ordering					
		When routing at minimum spacing route Alert between Data and Clock			

Main Func = CPU



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TitleCPU (VDDQ/VCC/VCCST)		
SizeA4	Document NumberEiffel-2_ICL_U	RevSA
Date: Friday, December 27, 2019	Sheet8	of106

Reserved

<Core Design>

<div>緯創資通</div>		<div>Wistron Corporation</div>			
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title					
CPU (RSVD)					
Size	Document Number		Rev		
A4	Eiffel-2 ICL U		SA		
Date:	Friday, December 27, 2019				
	Sheet	9	of 106		

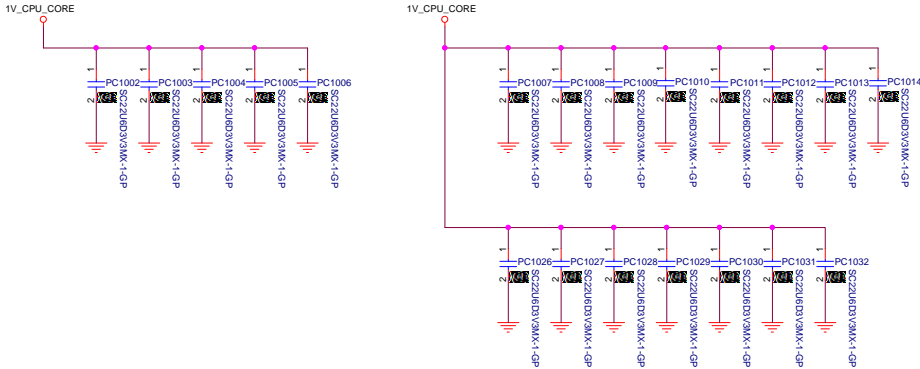
Main Func = CPU

VCORE

ICL_U42

U42
IccMax current-10ms max = 70 A

22uF	PCS	Cap
U42	15	330uF*2

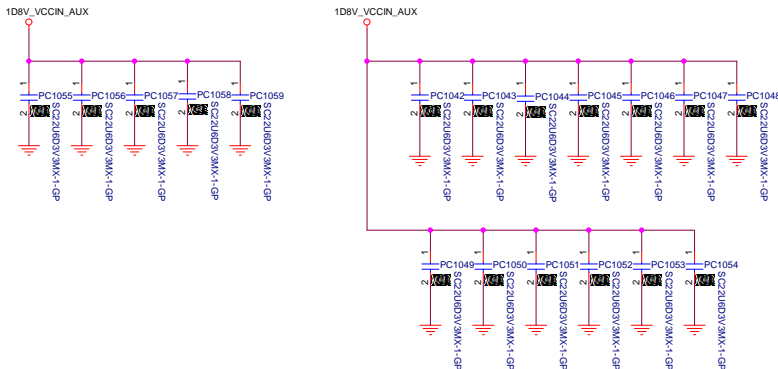


VCCINAUX

RT6543A

U42
IccMax 32A

22uF	PCS	Cap
U42	15	330uF*1



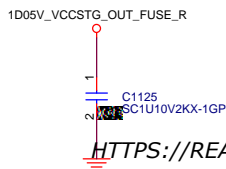
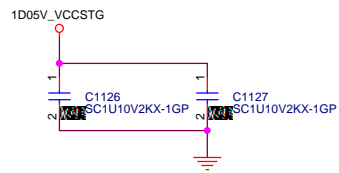
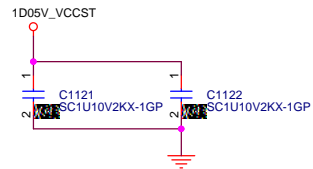
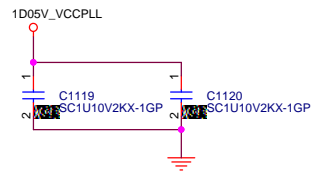
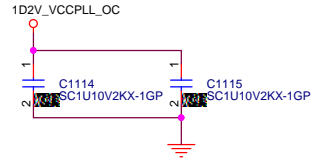
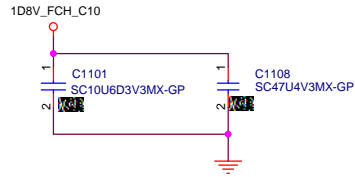
Decoupling Requirements for Ice Lake U Processor for VCCIN

Domain	Backside Cap	Primary Side Cap	Placement Guideline ²
VCCIN	4x 1uF 0402		Place directly underneath the group of pins close to BV36 or CT33.
	2x 10uF 0402		If placing on the backside, place directly underneath the group of pins close to V13. or If placing on the primary side, place close to the package edge near group of pins close to AB1.
	4x 22uF 0603		Place closest possible to package near heat sink mounting hole.
	6x 22uF 0603		Place closest possible to package along the plane breakout as in Figure below.
	3x 47uF 0805		Place closest possible to package near heat sink mounting hole.
	2x 330uF 7343		Refer to the placement guideline in Figure below.
Notes: 1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps > Power source. 2. Refer to the Figure below for decoupling capacitor placements.			

Decoupling Requirements for Ice Lake U Processor (Sheet 1 of 2)for VCCIN_AUX

Domain	Backside Cap	Primary Side Cap	Placement Guideline ²
VCCIN_AUX	12x 10uF 0402		Place them as directly below the BGAs as possible.
	7x 0402 (placeholder)		
		2x 220uF 7343	Place them close to VR.
		13x 10uF 0402	Place them close to the BGAs on the primary side.
		2x 22uF 0603	
Notes: 1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps > Power source. 2. Refer to the Figure below for decoupling capacitor placements.			

Main Func = CPU



Decoupling Requirements for Ice Lake U Processor for VCC1P8A

Domain	Backside cap	Primary side cap	Placement guideline ²
VCC1P8A		1x 10uF 0402 1x 0603 (placeholder)	Place as close to BGA as possible. Place this post power gate path to BGAs.

Notes:
1. Component placement order: Package edge > 0402 caps > 0605 caps > Bulk caps > Power source.
2. Refer to the Figure 11-9 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U Processor for VCCPLL_OC

Domain	Backside cap	Primary side cap	Placement guideline ²
VCCPLL_OC		1x 10uF 0402 1x 0402 (placeholder)	Place as close as possible to the package.

Notes:
1. Component placement order: Package edge > 0402 caps > 0605 caps > Bulk caps > Power source.
2. Refer to the Figure 11-12 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U Processor for VCCPLL

Domain	Backside cap	Primary side cap	Placement guideline ²
VCCPLL		1x 10uF 0402 1x 0402 (placeholder)	Place as close to the package as possible.

Notes:
1. Component placement order: Package edge > 0402 caps > 0605 caps > Bulk caps > Power source.
2. Refer to the Figure 11-14 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U Processor for VCCST

Domain	Backside cap	Primary side cap	Placement guideline ²
VCCST		1x 10uF 0402 1x 0402 (placeholder)	Place as close to the package as possible.

Notes:
1. Component placement order: Package edge > 0402 caps > 0605 caps > Bulk caps > Power source.
2. Refer to the Figure 11-16 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U Processor for VCCSTG

Domain	Backside cap	Primary side cap	Placement guideline ²
VCCSTG		1x 10uF 0402 1x 0402 (placeholder)	Place as close to the package as possible.

Notes:
1. Component placement order: Package edge > 0402 caps > 0605 caps > Bulk caps > Power source.
2. Refer to the Figure 11-18 for decoupling capacitor placements.

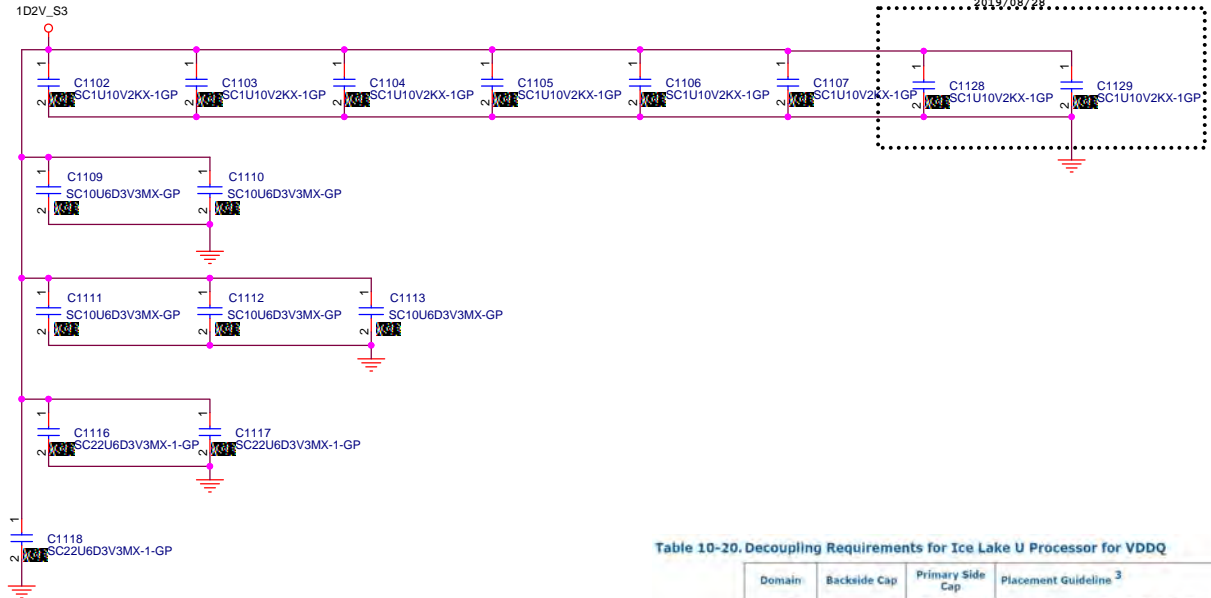


Table 10-20. Decoupling Requirements for Ice Lake U Processor for VDDQ

Domain	Backside Cap	Primary Side Cap	Placement Guideline ³
VDDQ		8x 1uF 0402	Place as close as possible to the SoC. The capacitor orientation should be horizontal with respect to the SoC edge. Use a shape to connect the capacitor to the VDDQ BGA, then use 2 uVias to from L1-L2 to connect the capacitor to GND. uVias should be placed as close as possible to the VDDQ pin of the capacitor.
		2x 10uF 0402	Place as close as possible to the SoC. The capacitor orientation should be horizontal with respect to the SoC edge. Use a shape to connect the capacitor to the VDDQ BGA, then use 2 uVias to from L1-L2 to connect the capacitor to GND. uVias should be placed as close as possible to the VDDQ pin of the capacitor.
		1x 0603 (placeholder)	Place after the DDR signal breakout.
		2x 22uF 0603	Place after the TOP DDR signal breakout. These should not be omitted on SODIMM designs, and can be removed only in Memory Down designs when the following conditions are met: 1) DRAM's are soldered down, so their decoupling is shared with the SoC. 2) DRAM's and SoC VDDQ plane copper is shared between both directly (no shorting resistors, pads or similar in the middle). 3) DRAM's are placed close to the SoC allowing that at least 5x10uF capacitors of the DRAM decoupling is within a 30mm radius from SoC Edge.

Notes:
1. Component placement order: Package edge > 0402 caps > 0605 caps > Bulk caps > Power source.
2. Refer to the Figure below for decoupling capacitor placements.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (Power Cap2)		
Size A3	Document Number	Rev
	Eiffel-2 ICL U	SA
Date: Friday, December 27, 2019	Sheet 11	of 106

M_A_ALERT_N
M_A_PARITY
V_SMA_VREF_CA
SM_DRANRST#

DQ00	DQ00-DQ7
DQ01	DQ8-DQ15
DQ02	DQ16-DQ23
DQ03	DQ24-DQ31
DQ04	DQ32-DQ39
DQ05	DQ40-DQ47
DQ06	DQ48-DQ55
DQ07	DQ56-DQ63

[illegible]

A circuit diagram showing a 5V supply connected to a resistor labeled R1231 240R2F-1-GP. The other end of the resistor is connected to the input of an op-amp labeled TS4A03MM1.

[illegible][illegible]

1	V185	V8
2	V185	V9
3	V185	V102
4	V185	V103
5	V185	V104
6	V185	V105
7	V185	V106
8	V185	V107
9	V185	V108
10	V185	V109
11	V185	V110
12	V185	V111
13	V185	V112
14	V185	V113
15	V185	V114
16	V185	V115
17	V185	V116
18	V185	V117
19	V185	V118
20	V185	V119
21	V185	V120
22	V185	V121
23	V185	V122
24	V185	V123
25	V185	V124
26	V185	V125
27	V185	V126
28	V185	V127
29	V185	V128
30	V185	V129
31	V185	V130
32	V185	V131
33	V185	V132
34	V185	V133
35	V185	V134
36	V185	V135
37	V185	V136
38	V185	V137
39	V185	V138
40	V185	V139
41	V185	V140
42	V185	V141
43	V185	V142
44	V185	V143
45	V185	V144
46	V185	V145
47	V185	V146
48	V185	V147
49	V185	V148
50	V185	V149
51	V185	V150
52	V185	V151
53	V185	V152
54	V185	V153
55	V185	V154
56	V185	V155
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88	V185	V187
89	V185	V188
90	V185	V189
91	V185	V190
92	V185	V191
93	V185	V192
94	V185	V193
95	V185	V194
96	V185	V195
97	V185	V196
98	V185	V197
99	V185	V198
100	V185	V199

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
DDR4 SODIMM 1DPC	VDDQ/ VDD	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)
		placeholder	1x 330 μ F (7343)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10 μ F (0603)
		Place on VTT plane close to DIMM	4x 1 μ F (0402)
	VDDSPD	DIMM pin side, 1 per DIMM	2x 10 μ F (0603)
		DIMM pin side, 1 per DIMM	2x 1 μ F (0402)
		1 cap per DIMM, Place close to DIMM	2x 0.1 μ F (0402)
		1 cap per DIMM, Place close to DIMM	2x 2.2 μ F (0402)

Note:
1. Total quantity is referring to 2 channels.

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wz Rd, Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR (DDR4 CHA)	
Doc ID:	Document Number: Eiffel-2 ICL_U
Date: Friday, December 27, 2019	
Sheet: 1-2 of 100	

Size Custom	Document Number Eiffel-2_ICL_U	Rev S
Date: Friday, December 27, 2019	Sheet 13 of	106

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24 PCH_DPWRCK <<< -
24,31,69 PLT_RST# <<< -
18,24,53 PM_SLP_SUSB# <<< -

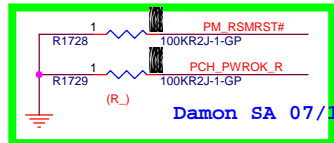
18,24,40,54,66 PM_SLP_S3# <<< -
18,24,34,40,66 PM_SLP_S4# <<< -
31 LAN_WAKE# <<< -

PM_PWRBTN# >>> -
ALL_SYS_PWRGD# >>> -
SYS_PWROK >>> -

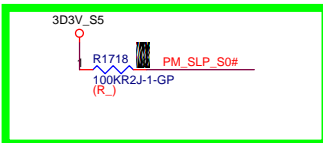
PCIE_WAKE# << >> - 61,63

VCCST_PWRGD >>> -
PCH_PWROK >>> -

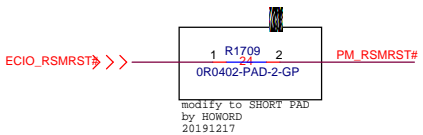
24,40 CPU_C10_GATE# <<< -



Damon SA 07/10



Follow Intel Recommend reserve 100k PU

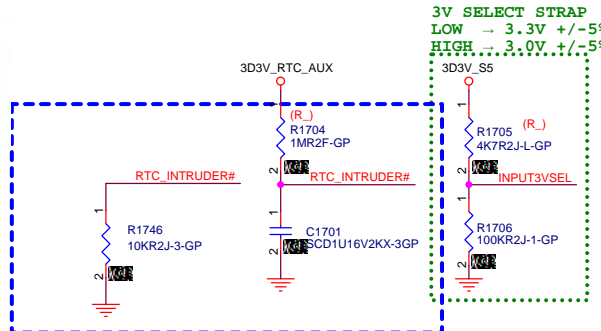
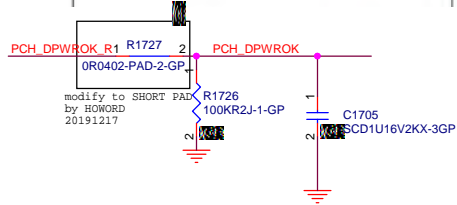


Damon SA 07/10

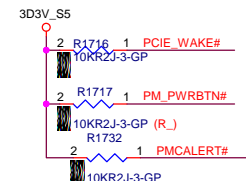
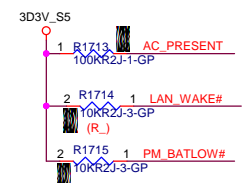
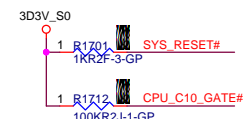
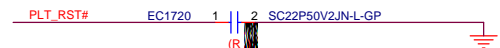
28.7 VCCSPI Voltage (3.3V or 1.8V) Selection

The VCCSPI voltage (3.3V or 1.8V) is selected via a hard strap on the RTCRST# pin. This strap sets the SPI interface signaling voltage at the rising edge of RTCRST#. Designers should strap this pin to match the expected interface operational voltage for their target SPI device as follows:
0 = SPI interface operation voltage is 3.3V (ground through a 10 kohm resistor)
1 = SPI interface operation voltage is 1.8V (pulled up with 1 Mohm to VCCRTC)

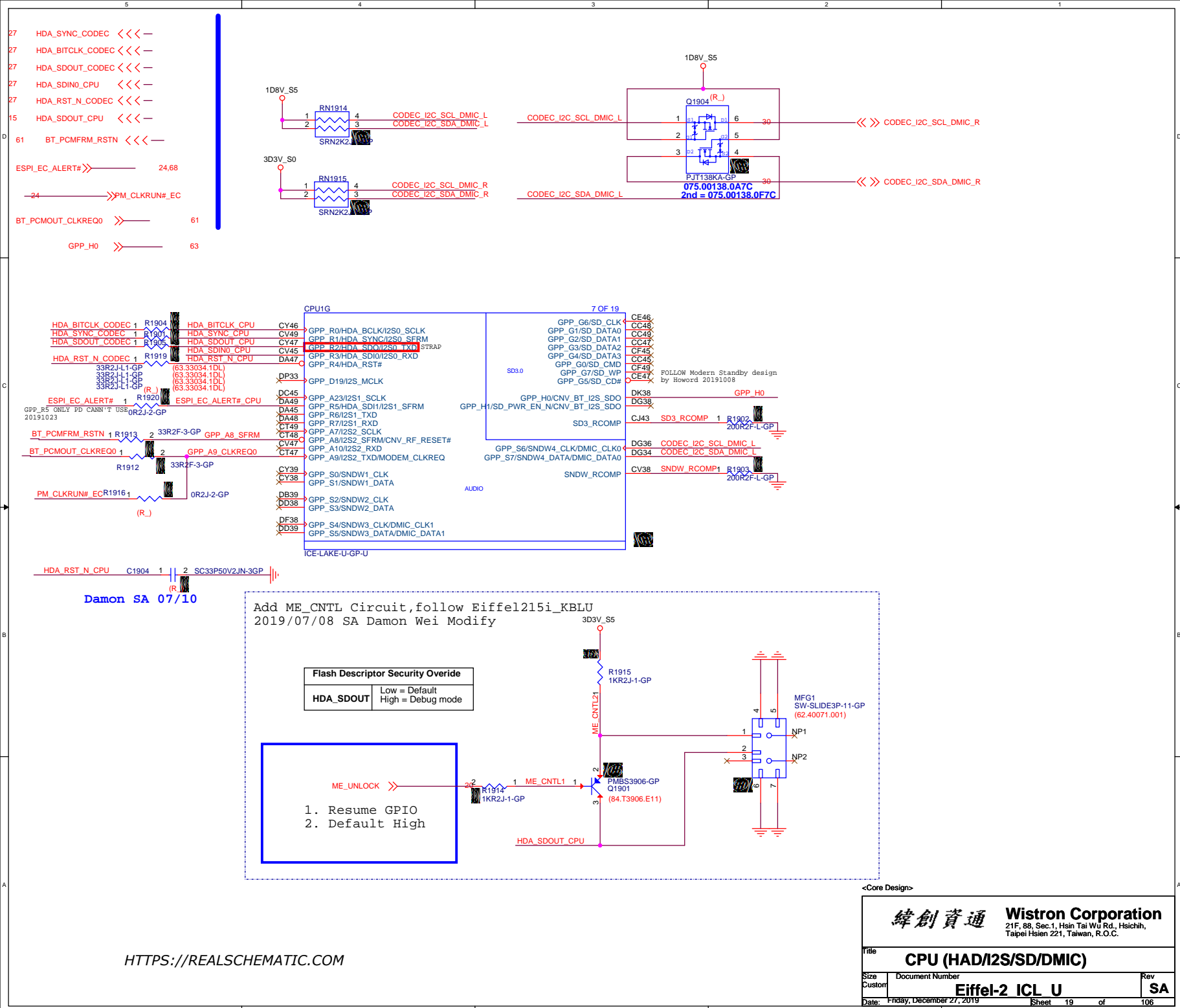
Figure 28-2. VCCSPI Voltage (3.3V or 1.8V) Selection



Howord SA modify 1001 follow PDG



Damon SA 07/10



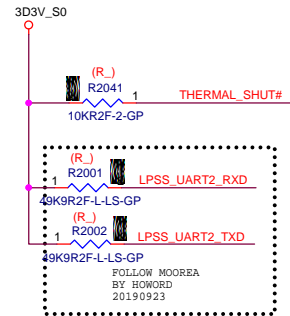
15 GSPI_MOSI
27 HDA_SPKR
15 SML1ALERT

RTC_DET# 25

EC_SMI# 24

LPSS_UART2_RXD 68

LPSS_UART2_TXD 68



GSPI_MOSI

HDA_SPKR

RTC_DET#

SML1ALERT

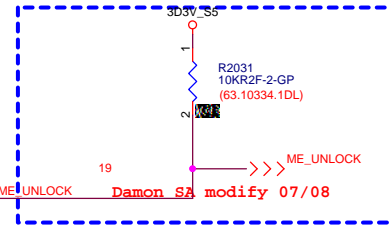
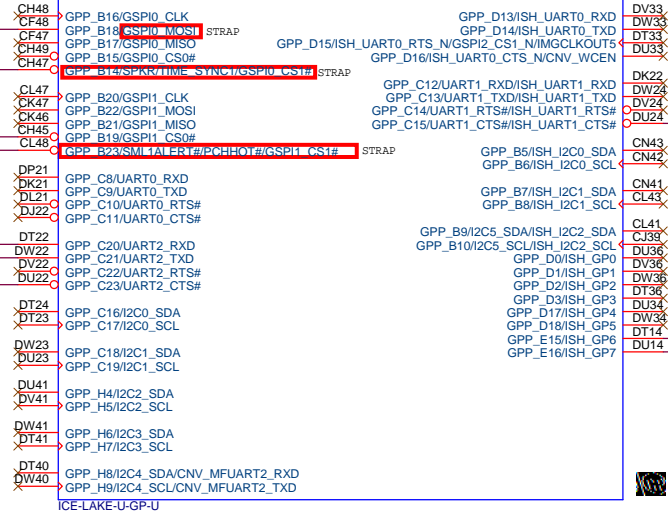
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LPSS_UART2_TXD

THERMAL_SHUT# 24

SMI/SCI_PIN

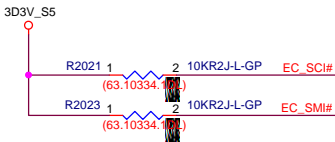
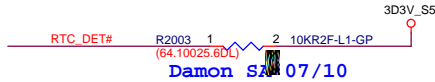
CPU1F 6 OF 19

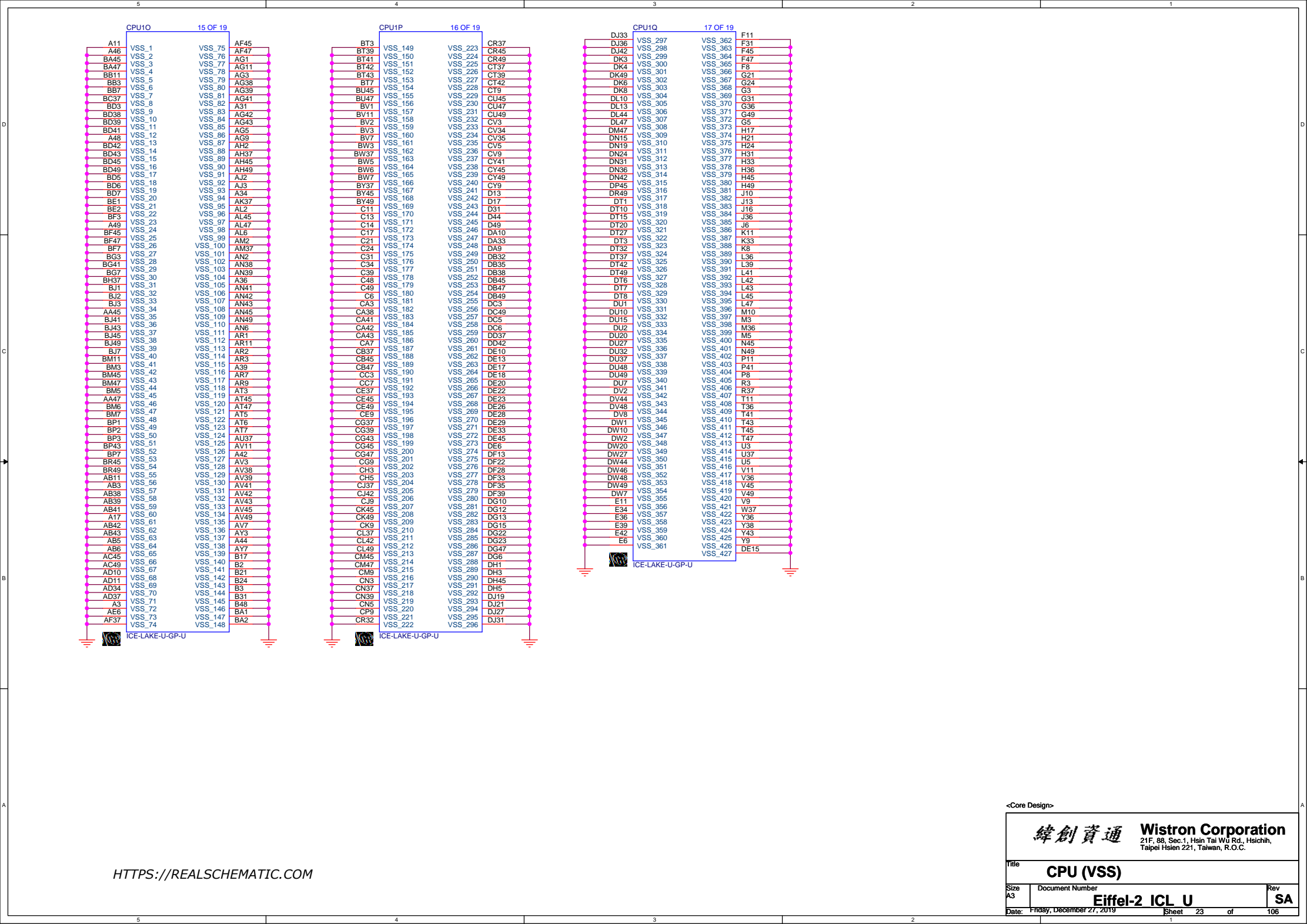


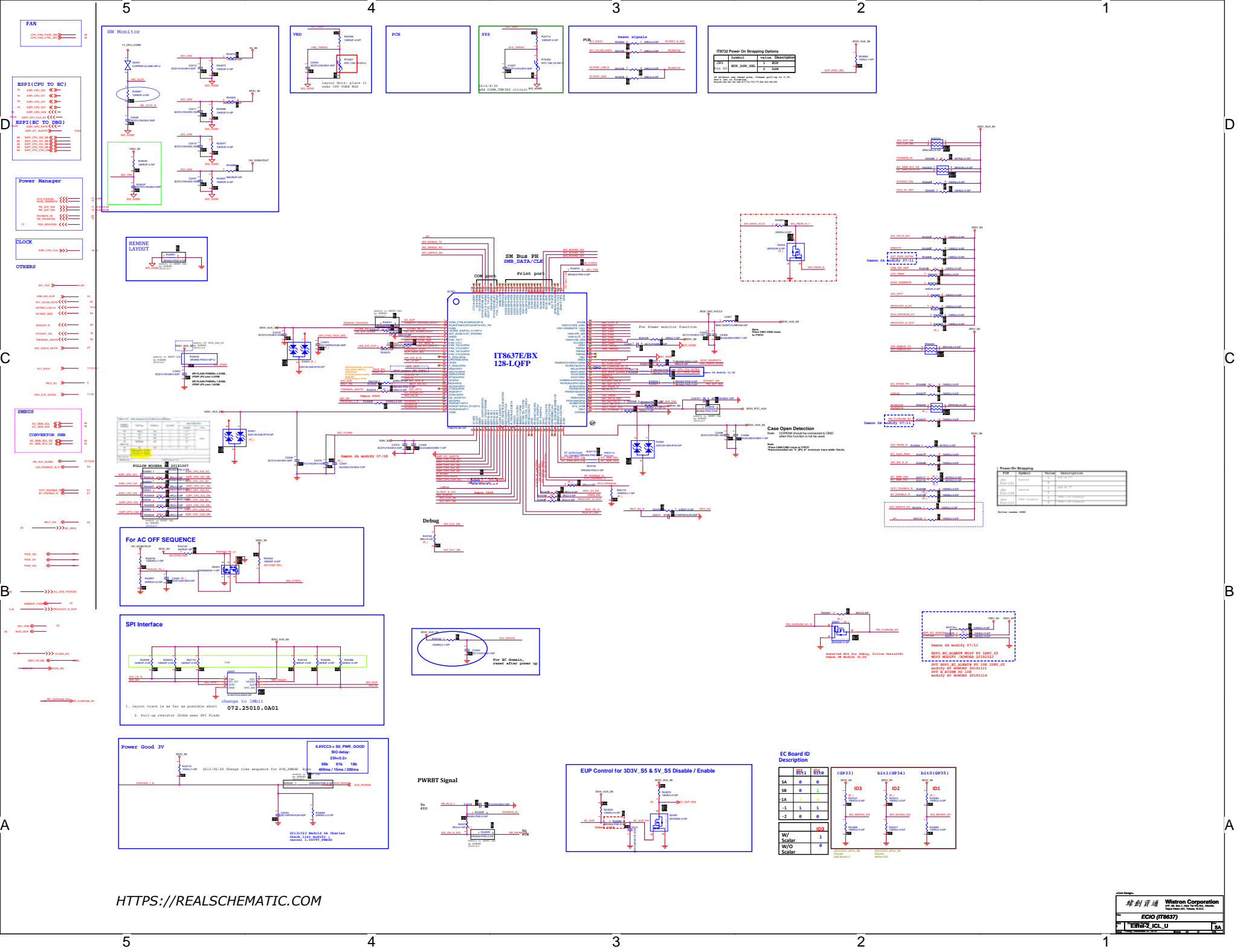
ME_UNLOCK
Damon SA modify 07/08

EC_SMI#

EC_SCI#



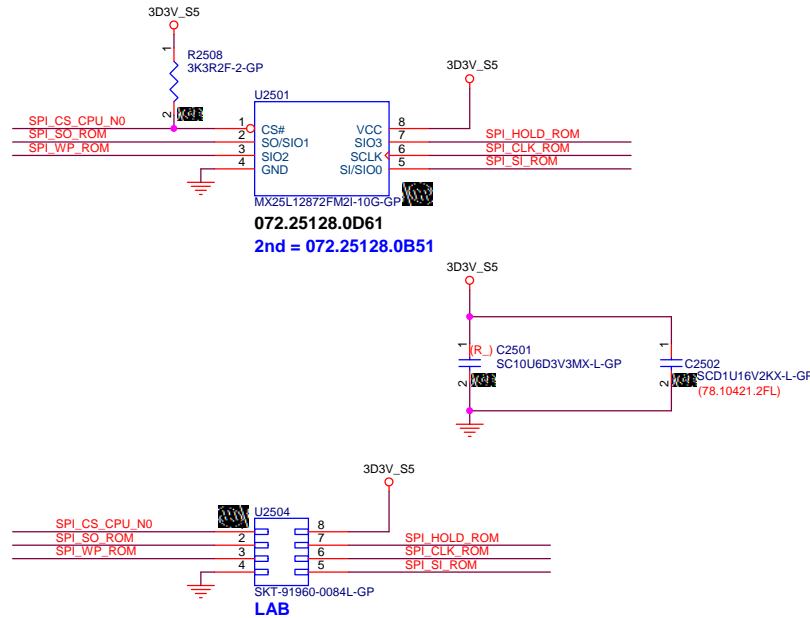




Main Func = SPI Flash

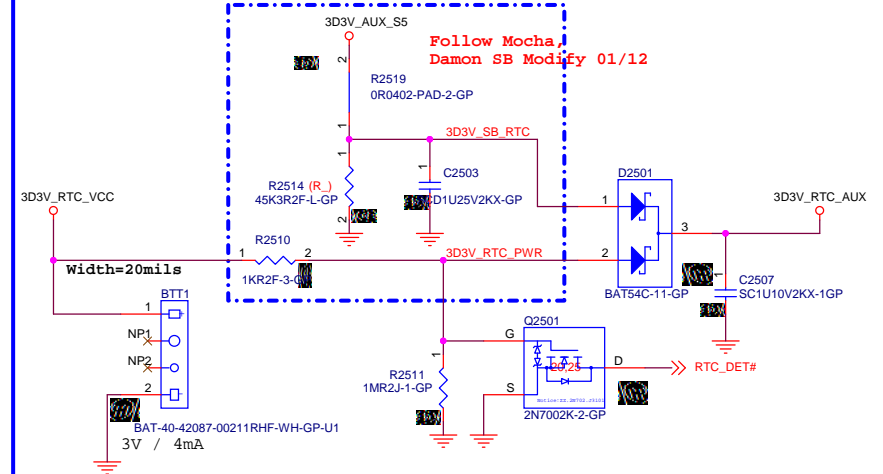
SPI FLASH ROM (16M byte) for PCH

SPI ROM Equal length need to less than 500mil



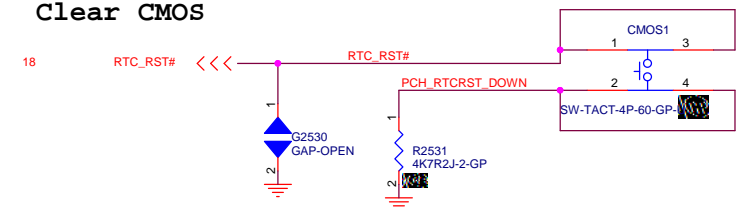
Main Func = RTC

RTC BATTERY



Change BTT1 CONN to (062.70001.0081), follow CE advice
Damon Wei SA Modify 2018/12/07

Clear CMOS



RTC Reset follow Eiffel215i_Kblu
Damon Wei SA Modify 2018/10/18

1-2 short :Clear CMOS
1-2 open : Normal (Default)

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Flash/RTC

Size

A3

Document Number

Eiffel-2_ICL_U

Rev

SA

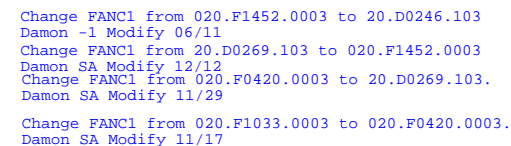
Date: Friday, December 27, 2019

Sheet

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of

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24
24

Title			
Flash/RTC			
Size B	Document Number		Rev
	Eiffel-2_ICL_U		SA
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Damon SB Modify 01/21



Title			
Audio (Codec_ALC256)			
Size	Document Number	Rev	
Custom	Effiel-2_ICL_U	SA	
Date:	Friday, December 27, 2019	Sheet	27 of 106

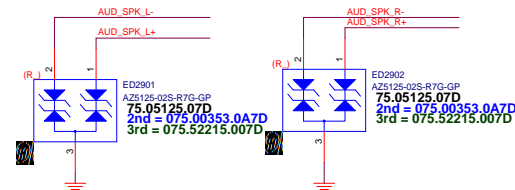
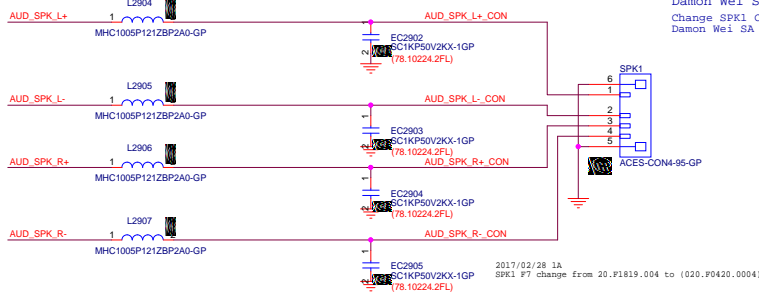
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SSID = AUDIO

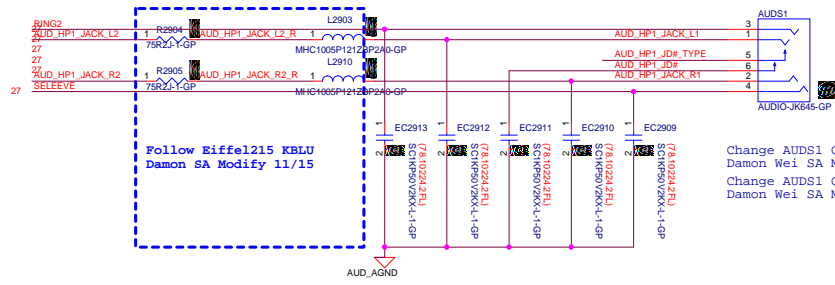
Speaker

2019/01/14 Damon SA Modify
L2904/L2905/L2906/L2907 change from 68.00335.151 to 68.00335.091 by P7

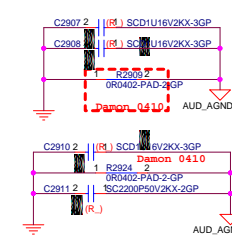
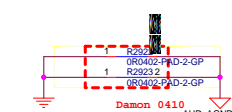
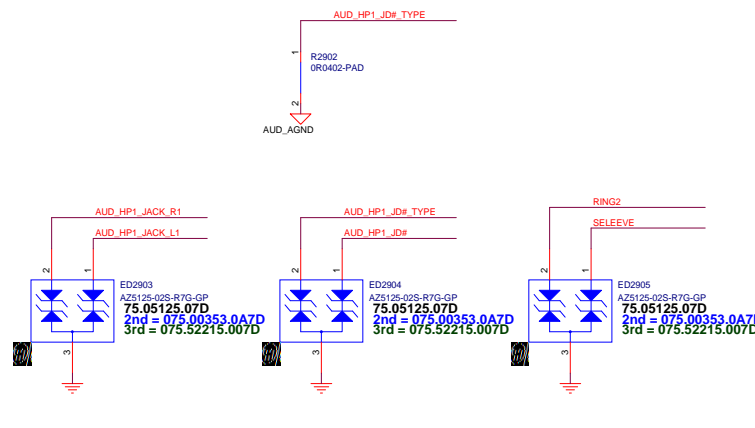
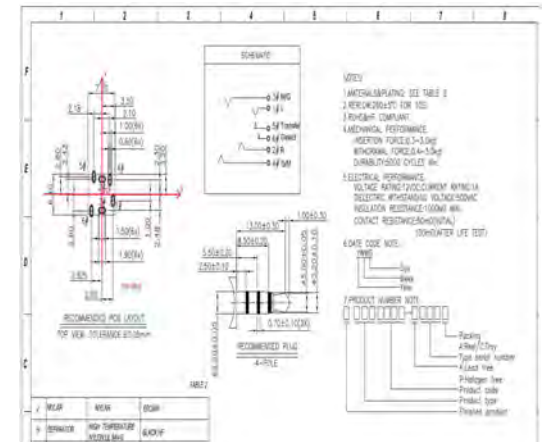
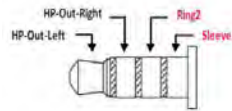
Change SPK1 CONN to 020.F0420.0004, follow Eiffel215_kblu.
Damon Wei SA Modify 2018/10/18
Change SPK1 CONN to 020.F1076.0004, follow CE advice
Damon Wei SA Modify 2018/12/07



RING2
AUD_HP1_JACK_L2
AUD_HP1_JD#
AUD_HP1_JACK_R2
SELEEVE
AUD_AGND



Change AUDS1 CONN to (022.10002.0C41), follow CE advice
Damon Wei SA Modify 2018/12/07
Change AUDS1 CONN to 022.10002.0K41, follow Eiffel215a.
Damon Wei SA Modify 2018/10/18



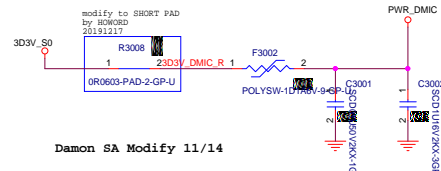
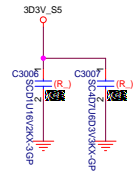
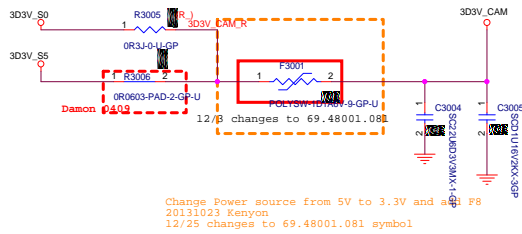
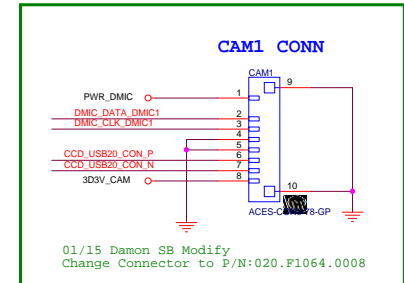
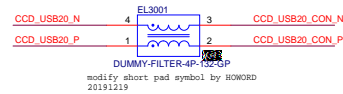
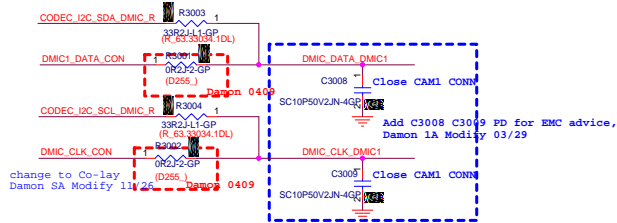
Follow Eiffel215 KBLU
Damon SA Modify 11/15

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DMIC

CODEC_I2C_SDA_DMIC_R 19
CODEC_I2C_SCL_DMIC_R 19
DMIC1_DATA_CON 27
DMIC1_CLK_CON 27

16 CCD_USB20_N
16 CCD_USB20_P



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Title Audio (RSVD)			
Size C	Document Number Eiffel-2_ICL_U	Rev SA	
Date: Friday, December 27, 2019	Sheet 30	of 106	

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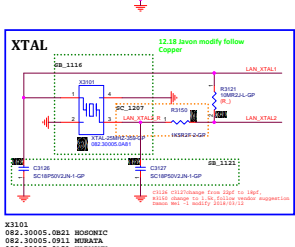
Giga LAN

PCI-E
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LAN_PCE_RX_P_C
LAN_PCE_TX_N_C
LAN_PCE_TX_P_C

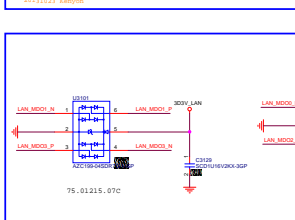
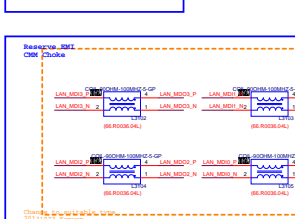
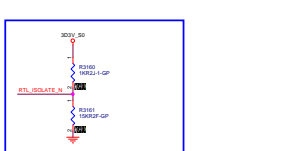
CLOCK
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LAN_CLK_CPU_P_C
LAN_CLKED_CPU_C

LAN
PCE_WAVEB
LAN_WAVEB
PLT_RSTB

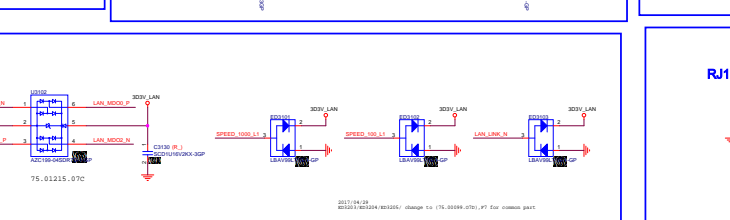
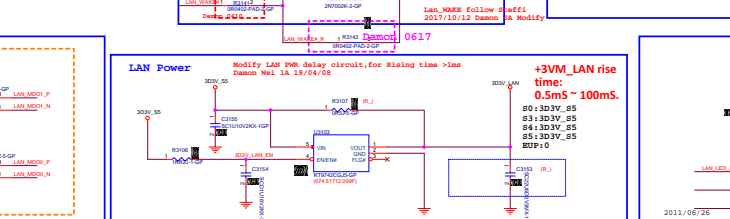
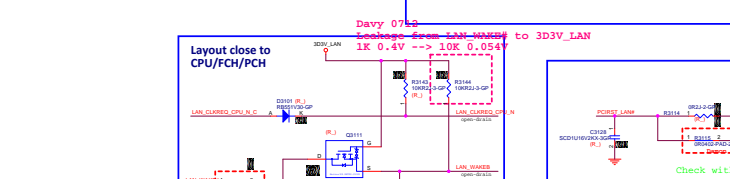
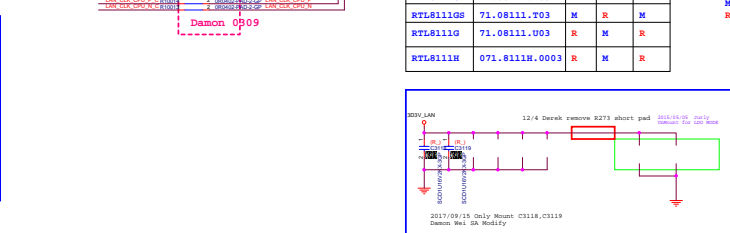
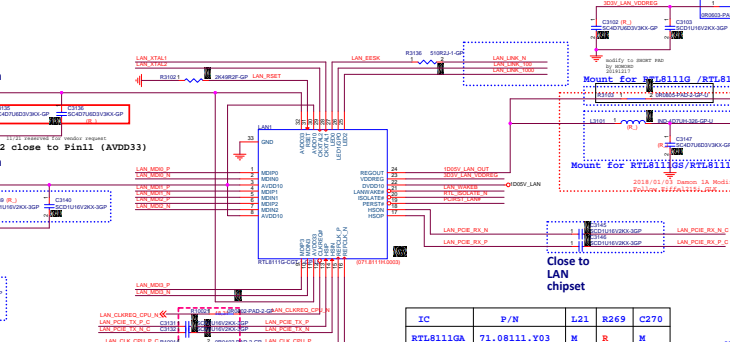
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Colse to the AVDD10 pin location
Colse to the pin22



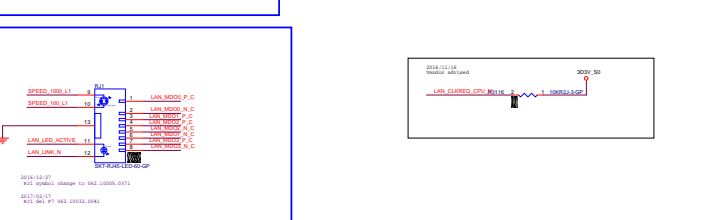
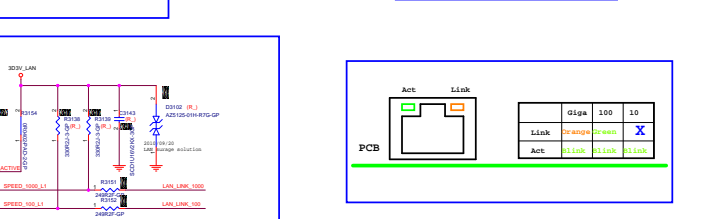
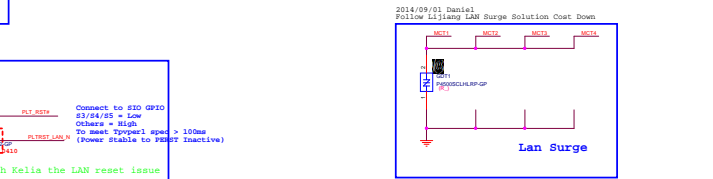
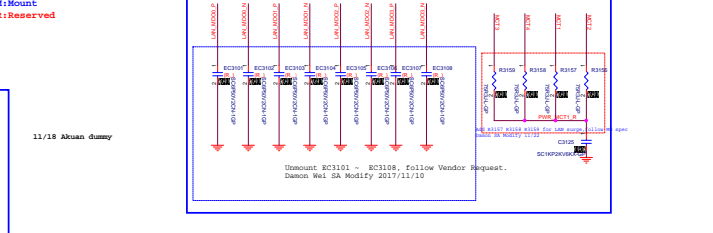
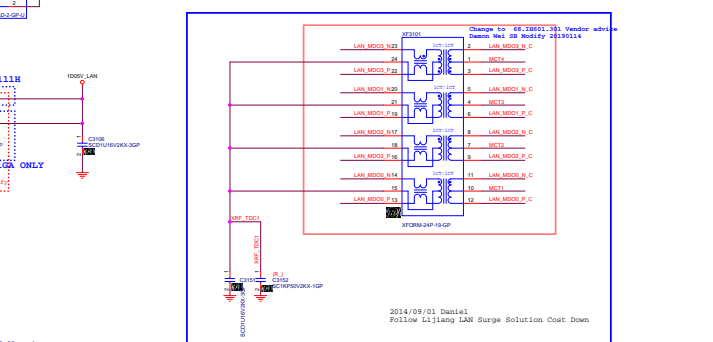
X3101
082.30005.0821 B080WIC
082.30005.0912 B080WIC
082.30005.0A81 B080WIC



75.01215.07C
75.01215.07C



2017/04/19
082101.00100.000000: change to 75.01215.07C for common part



2018/11/14
082101.00100.000000: change to 75.01215.07C for common part

Blanking

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN (RSVD) (RJ45+Trans)

Size
A4

Document Number

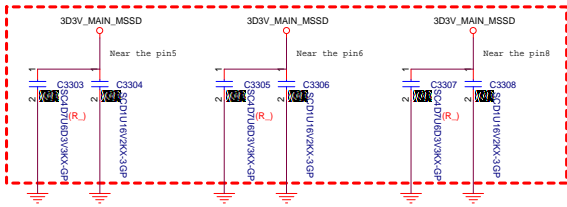
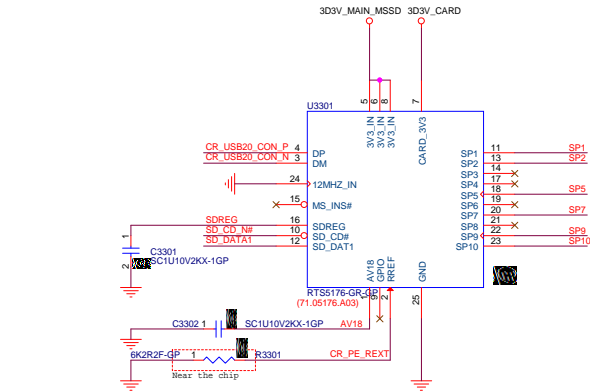
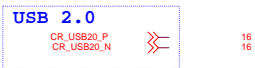
Eiffel-2_ICL_U

Rev
SA

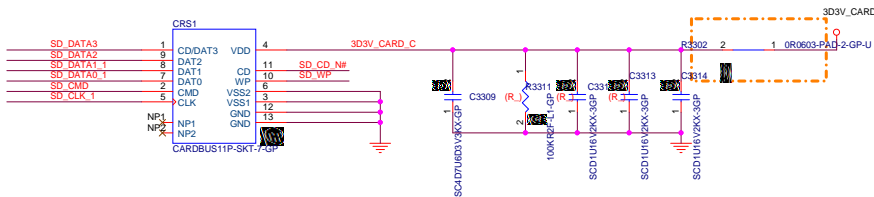
Date: Friday, December 27, 2019

Sheet 32 of 106

Card Reader



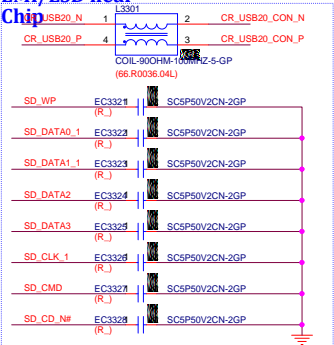
2IN1 CONN
(SD/MMC)



2IN1 (SD/MMC) Combo
Net



EMI/ESD near
Chip



RTD5176
Power



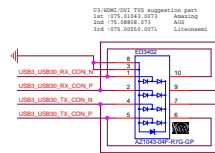
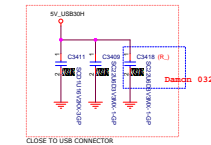
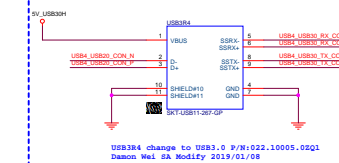
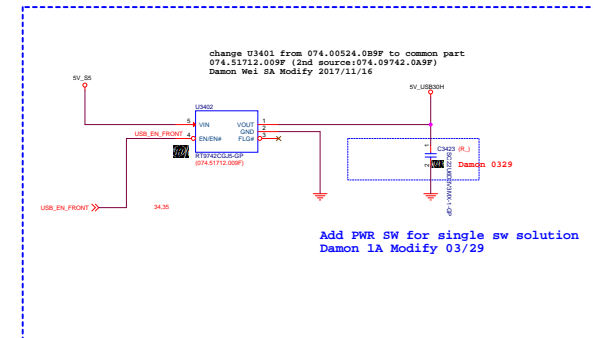
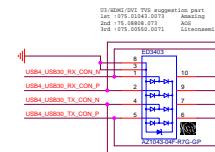
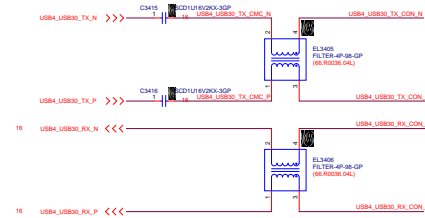
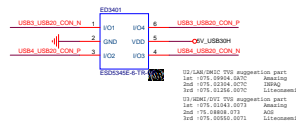
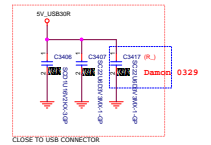
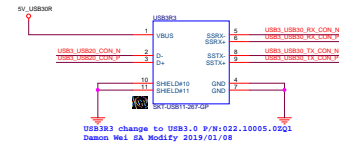
EMI
reserve



	S5	S4	S3-S0		S5	S4	S3-S0	Status
SLP S5 N	L	L	H	USB EN R	L	L	H	No Support S4/S5 USB wake up
USB SIO EUP	L/H	L/H	L	USB EN R	L	H	H	Support S4/S5 USB wake up

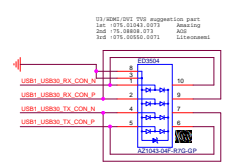
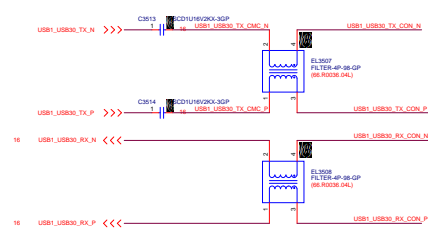
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The schematic diagram illustrates the USB3.0 interface circuit for the C3413 and C3414 modules. The C3413 module is connected to USB2_TX_N, USB2_TX_P, and USB2_RX_N. The C3414 module is connected to USB2_TX_P, USB2_RX_P, and USB2_RX_N. The USB3.0 hub is connected to USB3_TX_N, USB3_TX_P, USB3_RX_N, and USB3_RX_P. The hub is connected to the USB3.0 interface of the C3413 and C3414 modules.

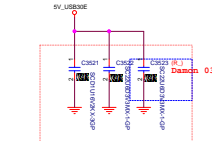
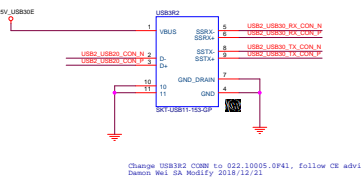
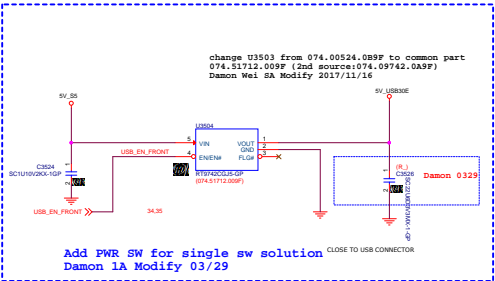
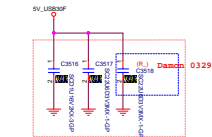
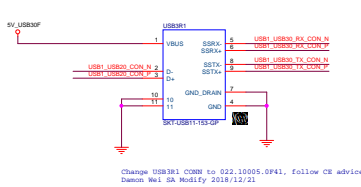
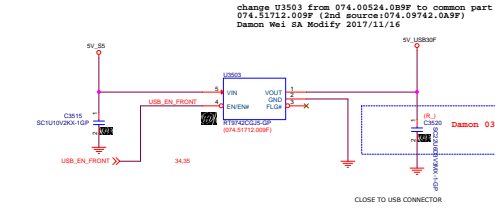
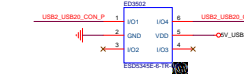
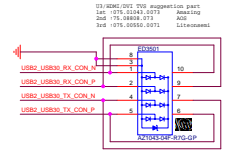
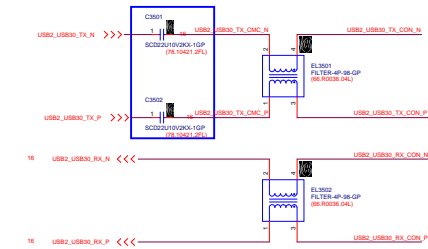
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Title USB (RSVD)				
Size	Document Number	Effeel-2_ICL_U		Rev
None	FW0001, 1/26/2011	Phase	34	106
		SA		

USB3.0 Side Port



Change to 220nf, follow PDG.
Damon Wei SA Modify 2018/10/18
Change to 100nf for USB1
Damon Wei SA Modify 2018/12/04



Reserved

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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (USB Charger)

Size

Document Number

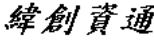
Rev

A3Eiffel-2 ICL USA

Date: Friday, December 27, 2019Sheet 36 of 106



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USB (RSVD)

Size
A3

Document Number
Eiffel-2 ICL U

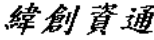
Rev
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Date: Friday, December 27, 2019

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Title

USB (RSVD)

Size
A3

Document Number
Eiffel-2 ICL U

Date: Friday, December 27, 2019


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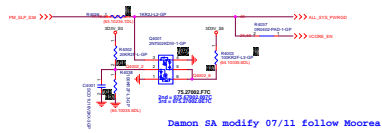
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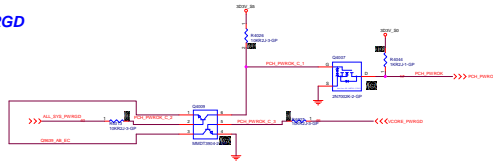
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Sequence (RSVD)			
Size A4	Document Number Eiffel-2_ICL_U		Rev SA
Date: Friday, December 27, 2019		Sheet 39	of 106

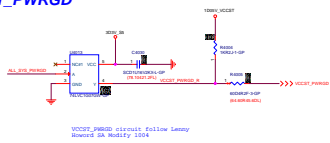
VCORE_EN



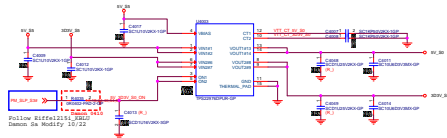
VCORE_PWRGD



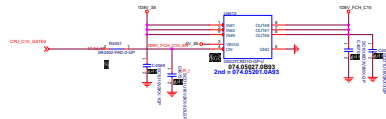
VCCST_PWRGD



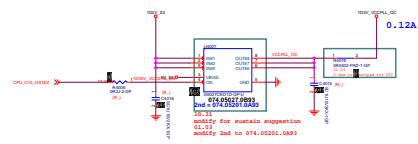
3D3V_S0 & 5V_S0



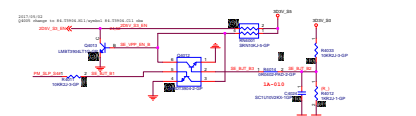
1D8V_FCH_C10



1D2V_VCCPLL_OC

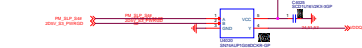


DDR4 Power Sequence

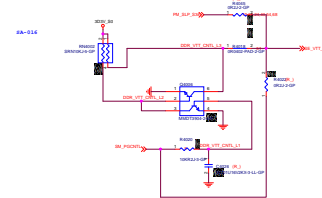


VPP(2.5V) enable

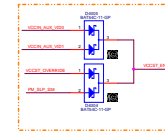
VDDQ(1.2V) enable



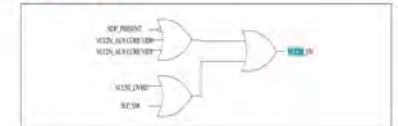
VTT(0.6V) enable



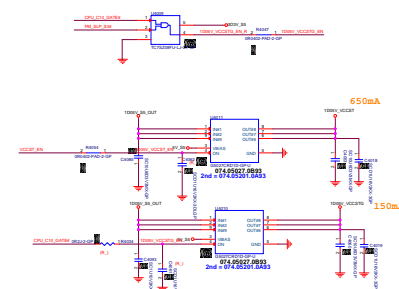
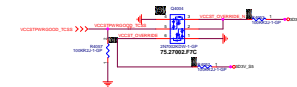
1D05V_VCCST_EN



11-17.VCCST Enable Logic



1D05V_VCCST/1D05V_VCCSTG





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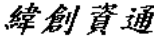
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Title		
Sequence (RSVD) (DS3/S0ix)		
Size A3	Document Number	Rev
Eiffel-2 ICL U		SA
Date: Friday, December 27, 2019	Sheet 41	of 106



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Title

INT IO (RSVD)

Size

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Rev

A3

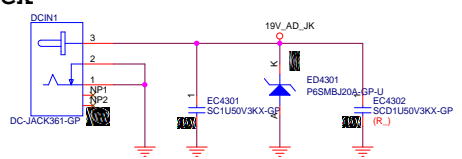
Eiffel-2 ICL U

SA

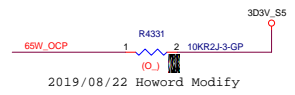
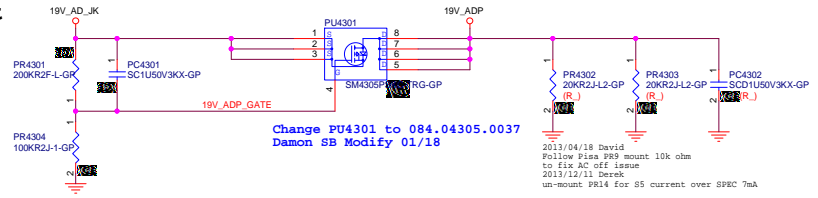
Date: Friday, December 27, 2019

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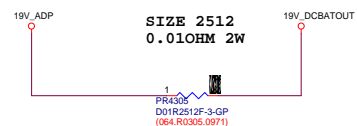
DC Jack



Soft start

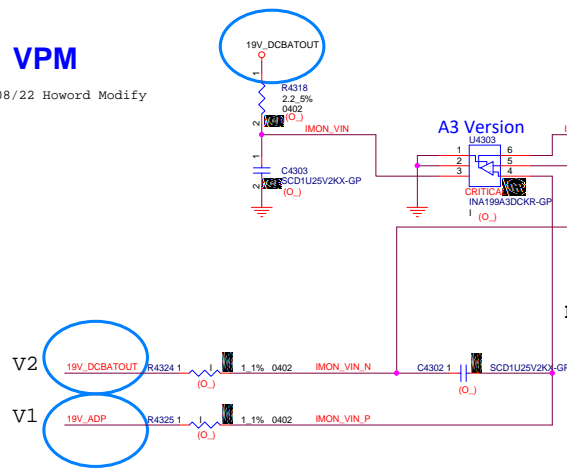


OCP

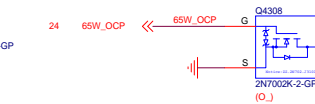


VPM

2019/08/22 Howard Modify



ECIO output GPO PIN27



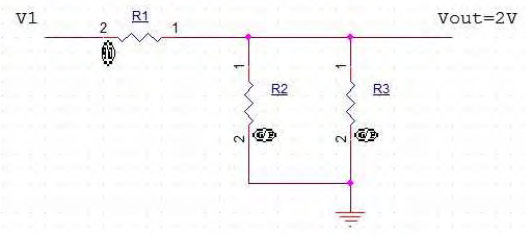
65W ADP
V=I*PR4101*gain
3.08*0.005*200=3.08V

90W ADP
V=I*PR4101*gain
4.26*0.005*200=4.26V

135W ADP
V=I*PR4101*gain
6.39*0.005*200=6.39V

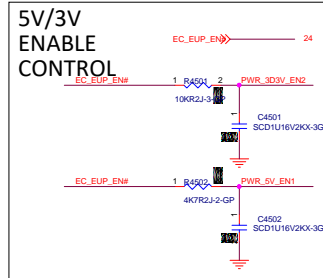
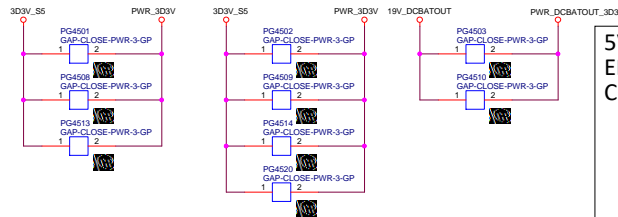
180W ADP
V=I*PR4101*gain
8.53*0.005*200=8.53V

ADP	180	135	90	65
I	9.47	7.11	4.74	3.42
OCP(I)	8.53	6.39	4.26	3.08
Gain	200	200	200	200
R	0.005	0.005	0.005	0.005
V1	8.53	6.39	4.26	3.08
PSYS	2	2	2	2
R1	100	100	100	100
R2	185.37	185.37	185.37	185.37
R3	36.71	60.32	168.89	0
Rth(R2/R3)	30.65	45.51	88.37	185.37

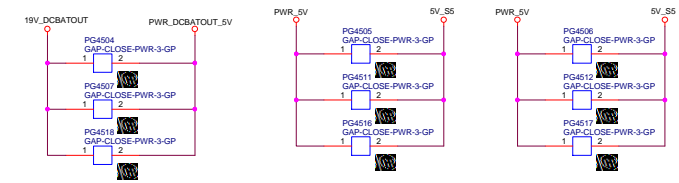


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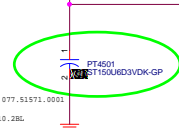
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5V/3V POWER GOOD



Iccmax=7.3A
OCP>10.95A



2017/02/16
Change P4501 to P080AP 077.51571.0001
2018/12/04
Change P4501 to T9.15710.28L

PWR_DCBATOUT_3D3V

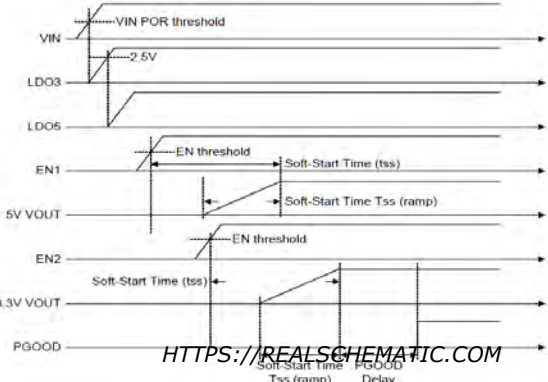
19V_DCBATOUT

PWR_DCBATOUT_5V

Iccmax=6.25A
OCP>9.375A

Change to 35K confirm with Power
Demon 68 Modify 01/18

$$V_{out} = 2 * (1 + R1/R2) = 5.0V$$



<Variant Name>

Figure 6. RT6575B Timing

PROCHOTn_CPU_R << 2 R4602 1 PROCHOTn_CPU
OR0402-PAD-2-GP

SVID_CLK_CPU << 2 SVID_CLK_CPU

SVID_DATA_CPU << SVID_DATA_CPU

SVID_ALERTn_CPU << SVID_ALERTn_CPU

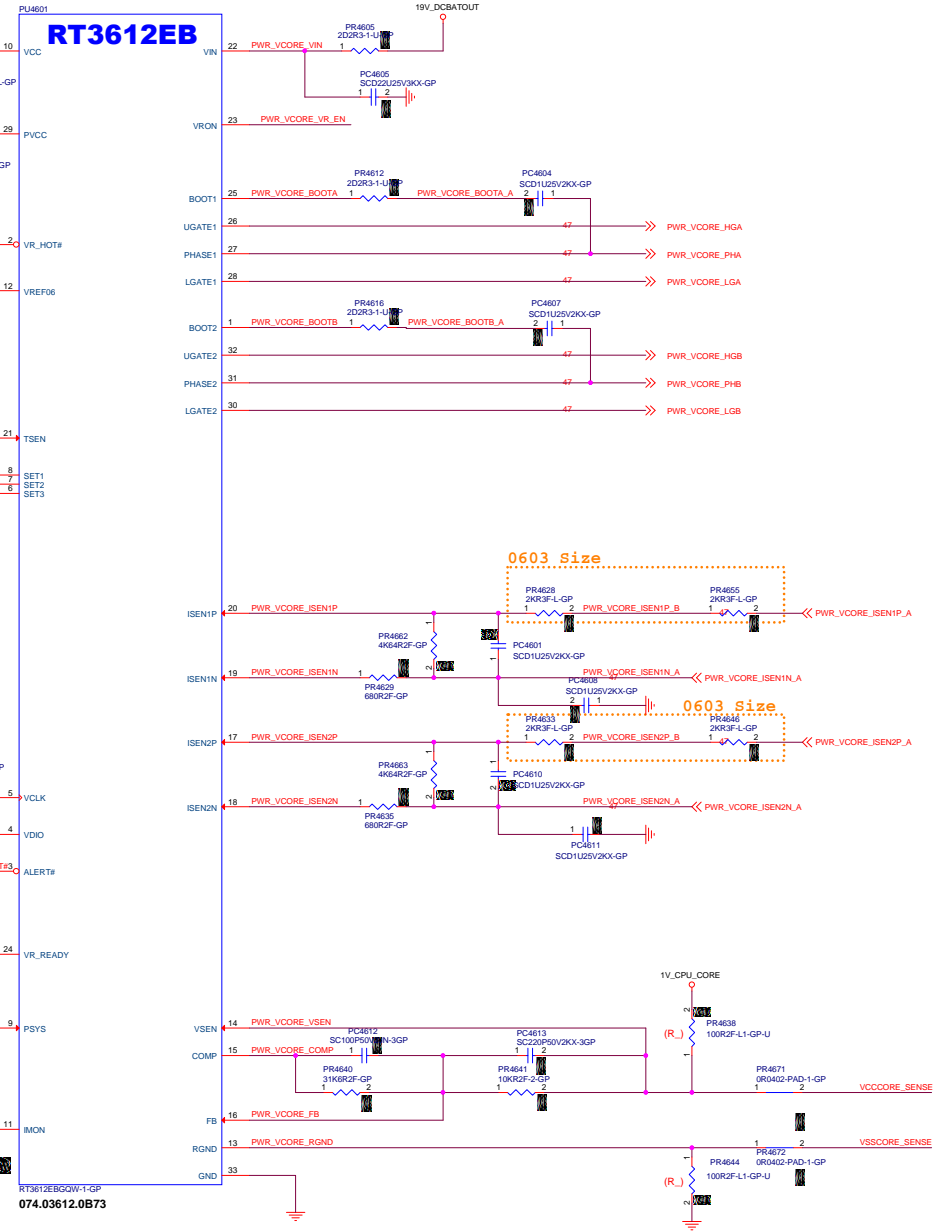
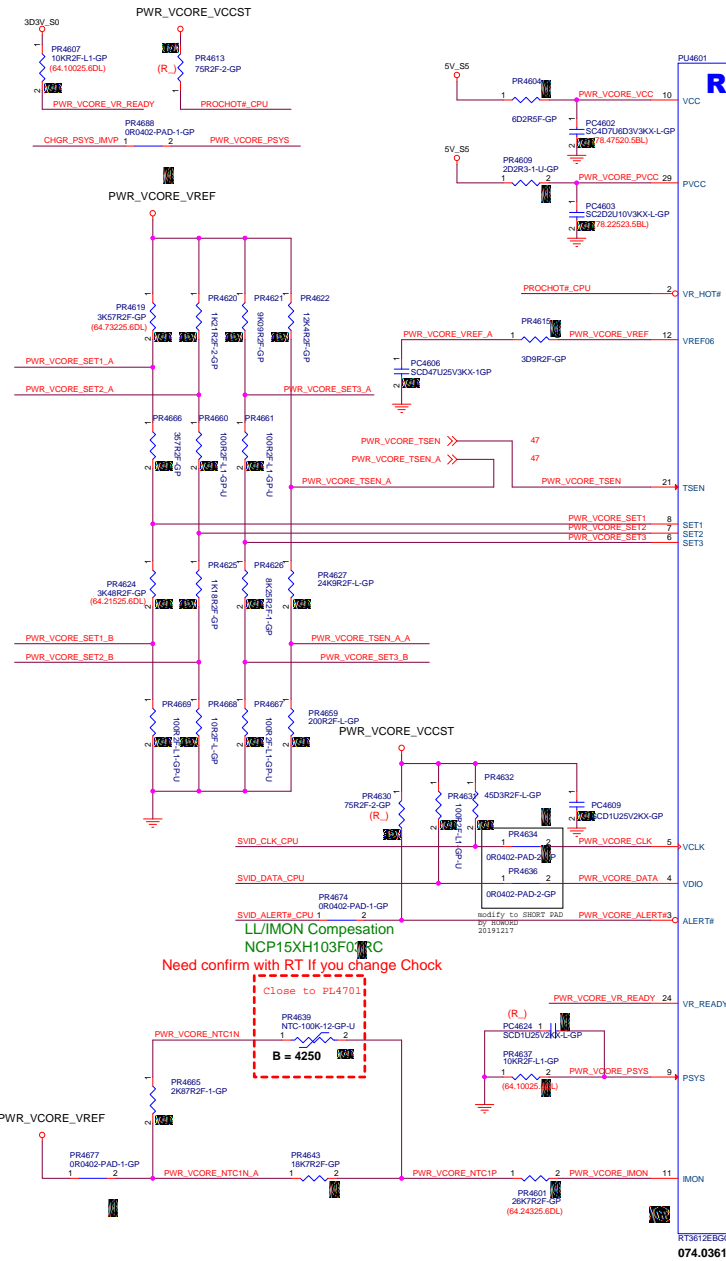
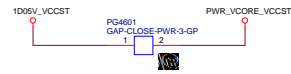
VSCORE_EN << VSCORE_EN 2 R4603 1 PWR_VCORE_VR_EN
OR0402-PAD-2-GP

VSCORE_PWIRG << VSCORE_PWIRG 2 R4604 1 PWR_VCORE_VR_READY
OR0402-PAD-2-GP

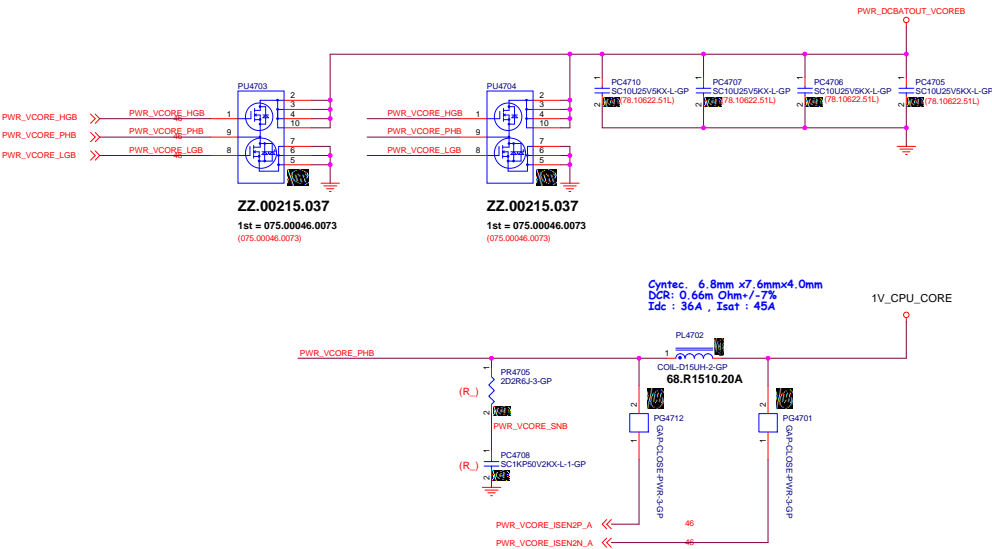
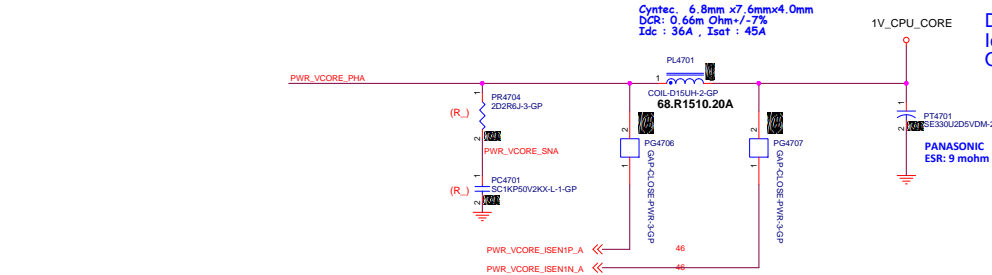
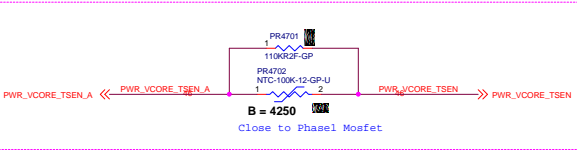
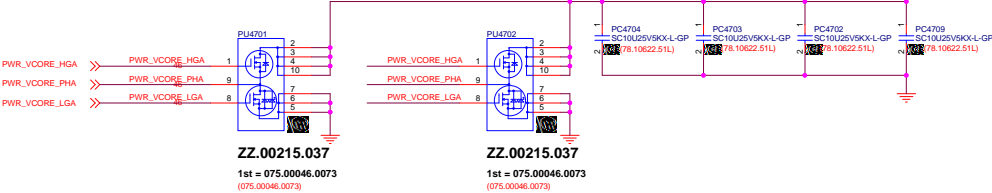
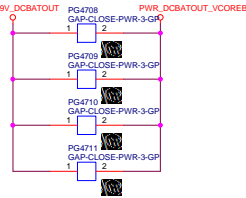
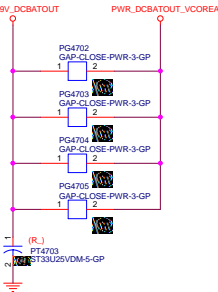
VSSCORE_SENSE << VSSCORE_SENSE

VCCORE_SENSE << VCCORE_SENSE

PSYS << 2 R4601 1 CHGR_PSYS_IMVP
OR023-3-GP



STD		緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File POWER (RT3613EE_VCORE(1/2))			
Size Custom	Document Number	Eiffel-2 ICL_U	Rev SA
Date	Friday, December 27, 2019	Sheet 48 of	108



Main Func = CPU_CORE

<Core Design>

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Title		
Power_CSD97396_CPU_VCCGT		
Size	Document Number	Rev
A2	Eiffel-2 ICL U	SA
Date	Friday, December 21, 2018	Sheet 48 of 108

The diagram illustrates the timing of the PWR_VCCAUX_PD signal. It shows the relationship between DEV_S0_PWRGD, PWRGD, PWRGD-PAD-1-GP, PWR_VCCAUX_EN, PWR_VCCAUX_PD, and PWR_VCCAUX_PD. It also shows the CPU side signals VCC0AUX_VBDI, VCC0AUX_VBDI, VCC0AUX_SENSE, VCC0AUX_SENSE, VSS0AUX_SENSE, and VSS0AUX_SENSE.

15V_DCBATOUT

PWR_DCBATOUT_VCCAUX

PG5001
GAP-C1-05E-PWR-R-3P
100nF
2

PG5002
GAP-C1-05E-PWR-R-3P
100nF
2

PG5003
GAP-C1-05E-PWR-R-3P
100nF
2

PG5004
GAP-C1-05E-PWR-R-3P
100nF
2

R1
10k

R2
10k

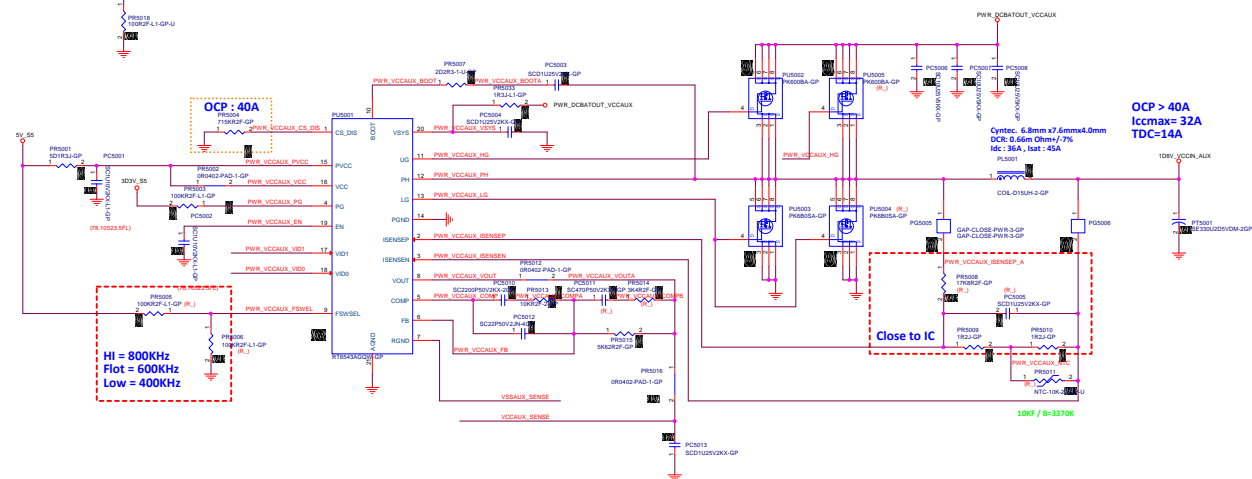
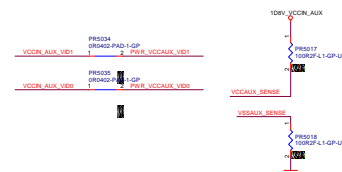
R3
10k

R4
10k

1.2V

PG5002
P72022

PG5003/25VDM-5-GP



SSID = PWR.Plane.Regulator_1p2v0p6v

VDDQ
POWER
GOOD

VDDQ
ENABLE
CONTROL

VDDQ_EN >>> 24,40,51,52

2017/04/19
P85127 change to short pad

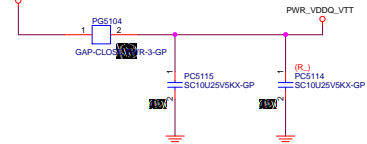
Freq. setting
750K -> 350K Hz

Need EE confirm

VDDQ_EN >>> VDDQ_EN 24,40,51,52
P85113 2
SC-027
SC-037
P85110
SCD1U16V20K-L-GP
2017/04/19
P85114 change to short pad

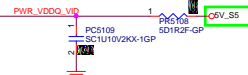
SE_VTT_EN >>> P85112 2
OR0402-PAD-2-GP
P85116
SC1U10V20K-L-GP
P85114
SC1U10V20K-L-GP

Vout =
0.6V
Iomax =
0.75A
IDDV_VREF_S0

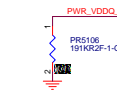


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VID
Logic-High = 0.75V
Logic-Low = 0.3V



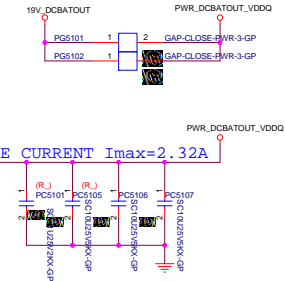
OCP setting



84.04C10.037 NTMP84C10N
Rds(on) = 5.8-6.95 mohm,
Vgs=10V, I-D = 30A,
Qg = 18.9nC
Vgs=10V, Vds=15V, I-D=30A

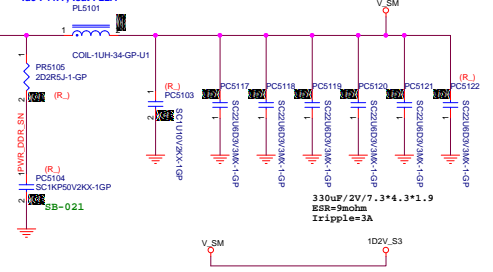
84.04C06.037 NTMP84C06N
Rds(on) = 3.2-4.0 mohm,
Vgs=10V, I-D = 30A,
Qg = 29nC
Vgs=10V, Vds=15V, I-D=30A

VIN RIPPLE CURRENT Imax=2.32A

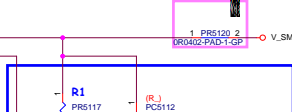


Cymtec. 6.8mm x7.3mmx3.0mm
DCR: 9m - 10m Ohm
Idc: 11A, Istat: 22A
PL5101

I_{design}=9.5A
14.25A<OCP<19A



Close to output cap pin1, not inside of the output cap



Vout Setting
Vout = Vref * (1 + R1/R2)
= 0.675 * (1 + 15.8K / 20K)
= 1.2V

VID vs Vref Table
VID Logic-High => Vref = 0.675 V
VID Logic-Low => Vref = 0.75 V
note: Vref can only be changed from
0.675v to 0.75v after power-on

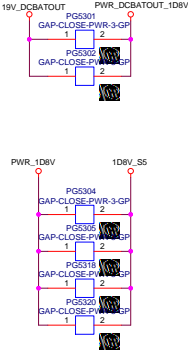
<Variant Name>

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File POWER MEM&VTT RT8231A 1D2V	
Size	Document Number
Customer	Eiffel-2 ICL U
Date: Hsinyi, December 27, 2010	Sheet 51 of 159

2D5V
POWER
GOOD



OFFPAGE_GAP

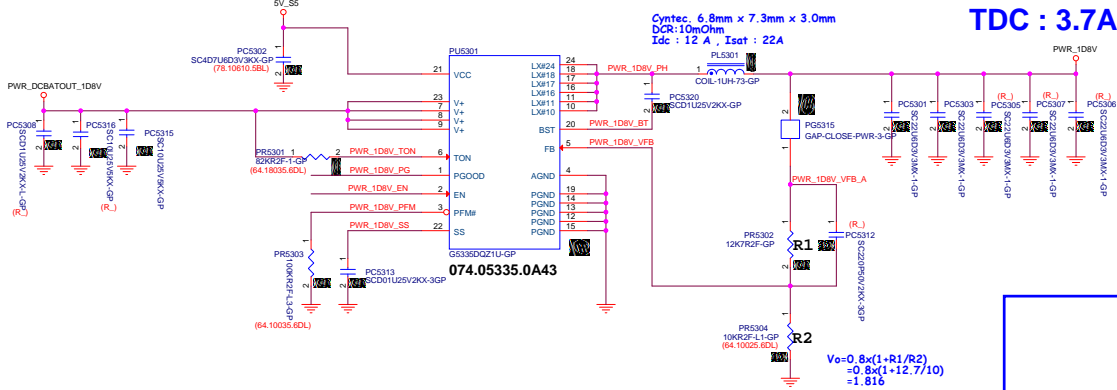


SSID = PWR.Plane.Regulator_1p0v

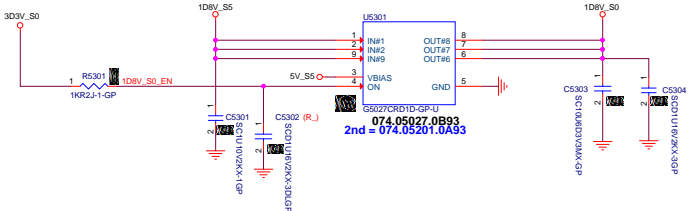
G5335D for 1D8V

Cyntec, 6.8mm x 7.3mm x 3.0mm
DCR:10mOhm
Idc : 12 A , Isat : 22A

TDC : 3.7A



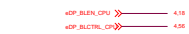
1D8V_S5 to 1D8V_S0



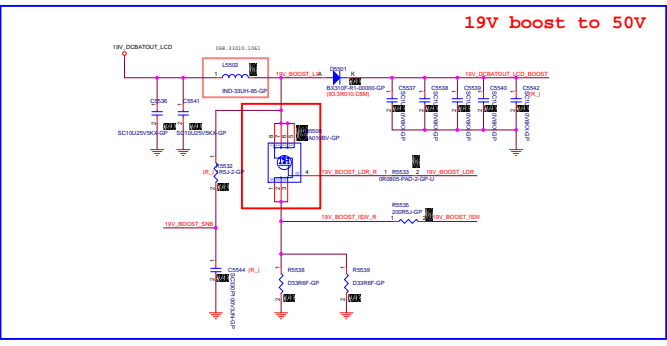
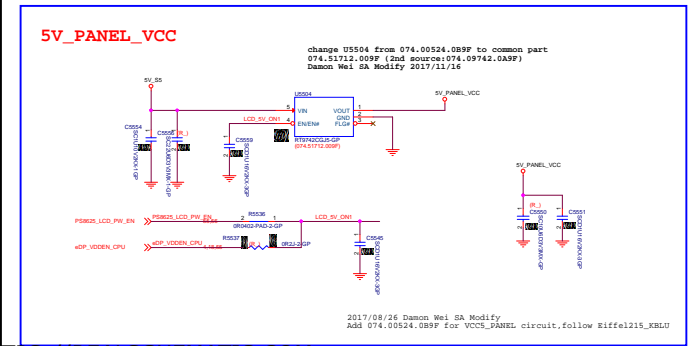
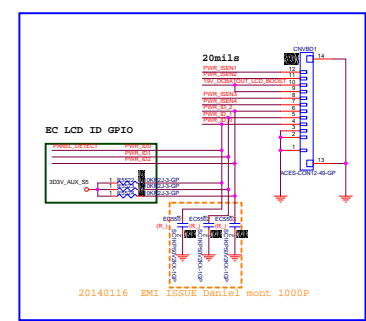
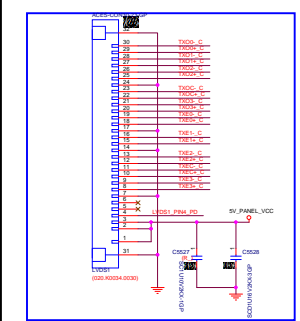
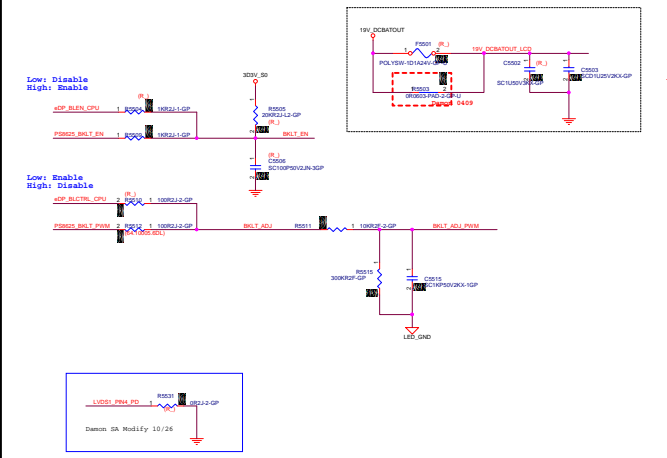
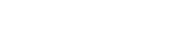
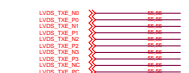
LCD ID



LVDS For Scalar



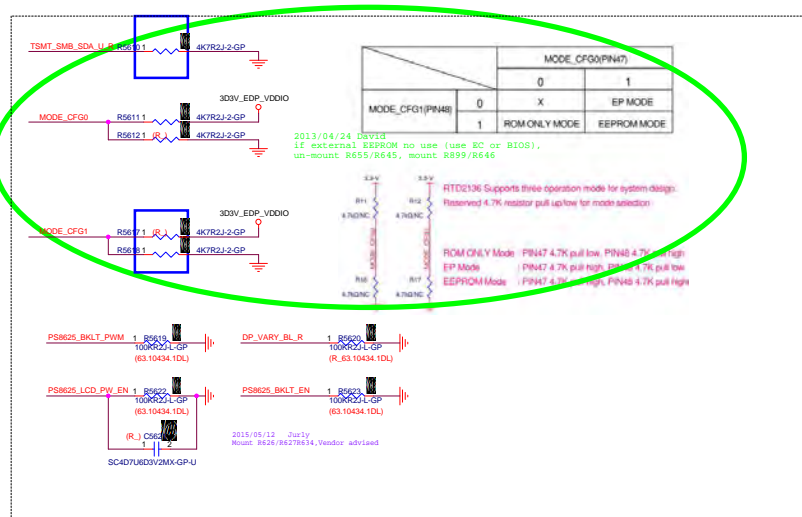
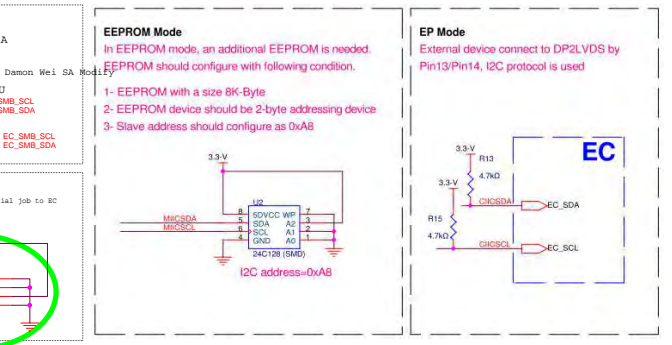
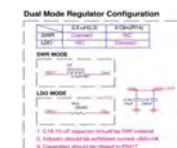
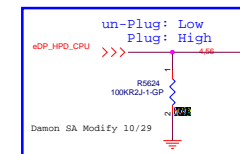
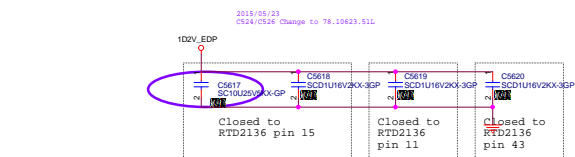
LVDS For eDP translator



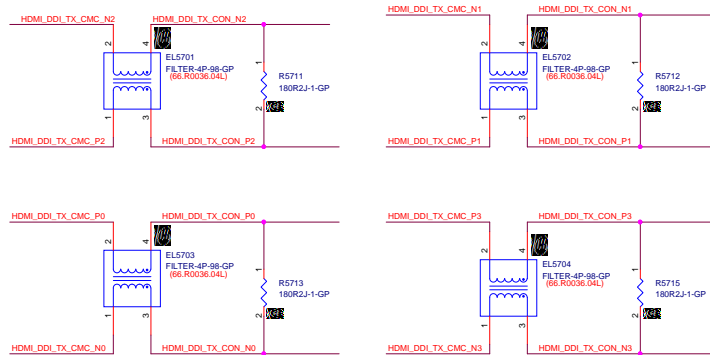
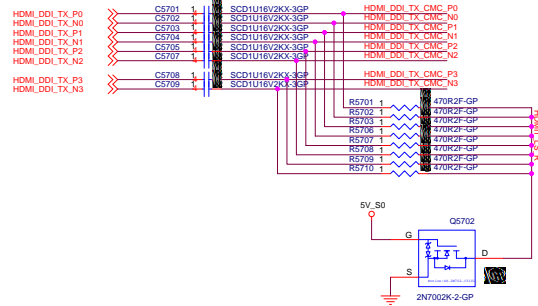
Panel Model	ID0	ID1	ID2	Vout
LG LM230WF3-SLK1	0	0	0	3.4 Vout 1.6 RTN 2.5NC
LG LM230WF5-TLF1	0	0	1	3.4 Vout 1.6 RTN 2.5NC
LG LM230WF3-SLL1	0	1	0	3.4 Vout 1.6 RTN 2.5NC
CMi M195FGE-L20 C1	1	0	0	1.2,5.6 Vout 3.4 RTN
CMi M195FGE-L20 C3	1	1	0	1.2,5.6 Vout 3.4 RTN
CMi M195FGE-L20 C1	1	1	1	1.2,5.6 Vout 3.4 RTN

Modified by Kenyon. Use CMC to choose signal source. 2012/11/07

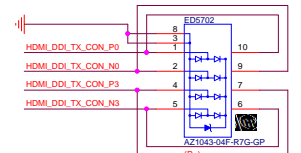
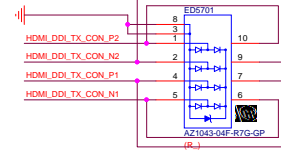




HDMI V1.4b

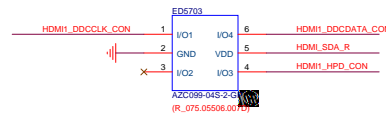


U3/BDML/DVI TVS suggestion part
1st : 075.0103.0073 Anazing
2nd : 075.0808.073 AGS
3rd : 075.0050.0073 Liteonsemi



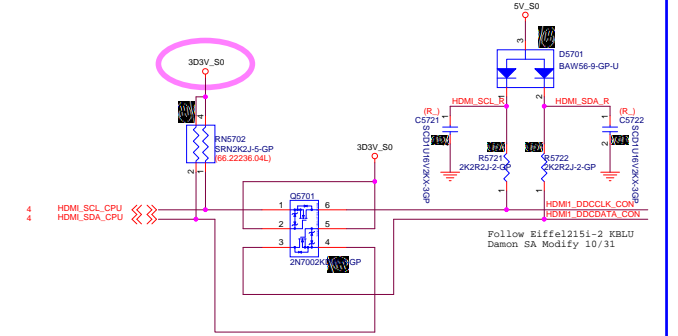
U2/LAN/GMIC TVS suggestion part
1st : 075.09904.0A7C Anazing
2nd : 075.02304.0C7C IRPAQ
3rd : 075.01256.007C Liteonsemi

use 5V_DDC_RDM1
To prevent leakage

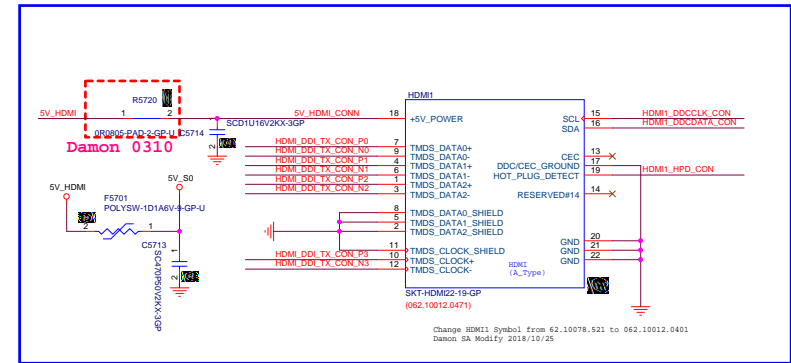


HDMI DDC Level Shift

D5701 change from 75.00056.D7D to 75.00056.07D, because OBS.Damon SA Modify 11/15



Follow Eiffel2151-2 KBLU
Damon SA Modify 10/31

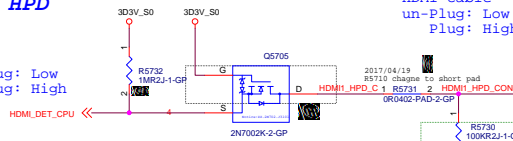


Change HDMI1 Symbol from 62.10078.511 to 062.10012.0401
Damon SA Modify 2018/10/25

HDMI HPD

un-Plug: Low
Plug: High

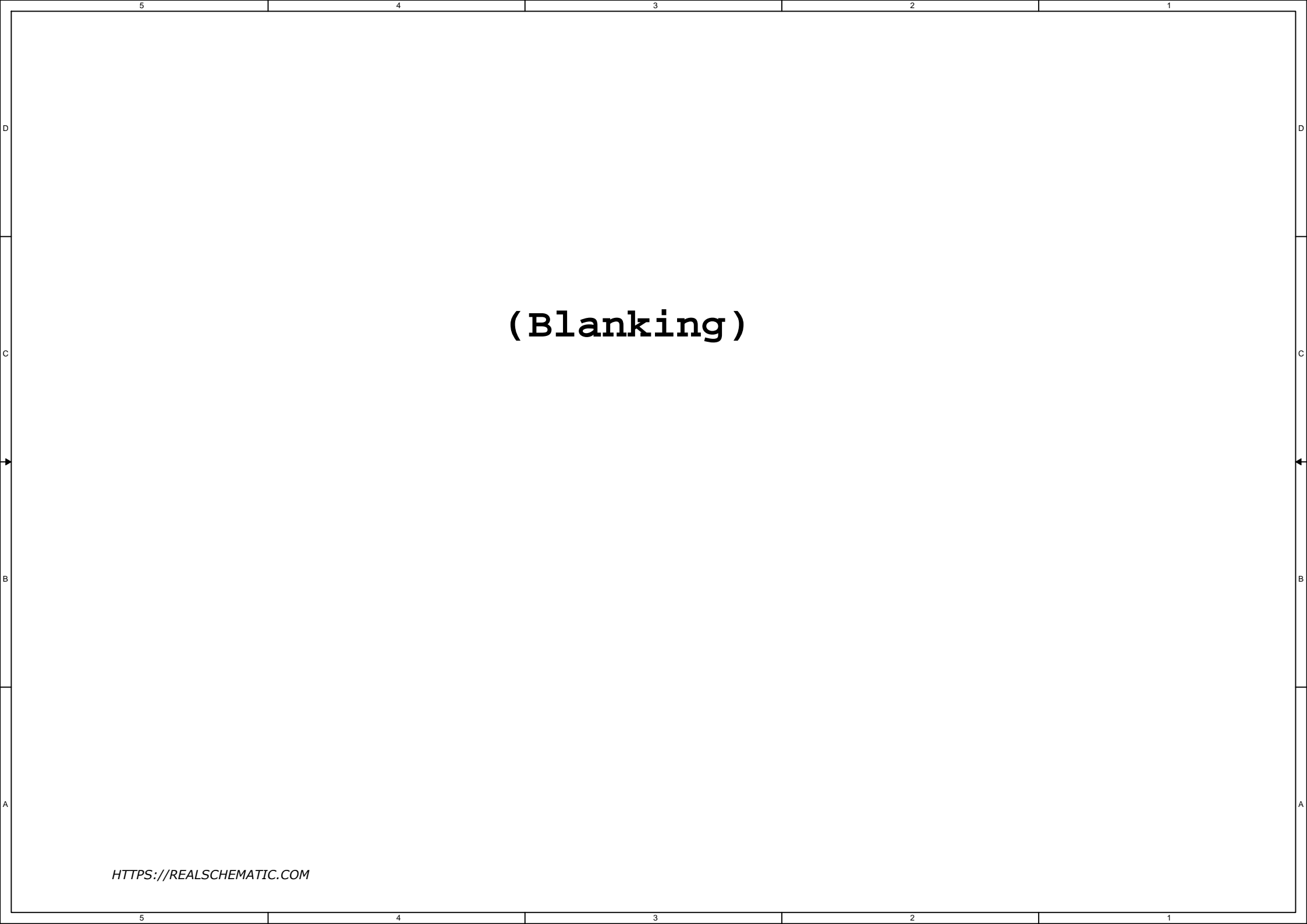
HDMI cable
un-Plug: Low
Plug: High



Follow Eiffel2151_KBLU
Damon SA Modify 10/29

<Variant Name>

緯創資通 Wistron Corporation		21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
File		Display (HDMI/Conn)	
Size	Document Number	Eiffel-2_ICL_U	
Rev	SA	108	
Date: 10/25/2018		Rev: 01	

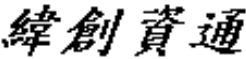


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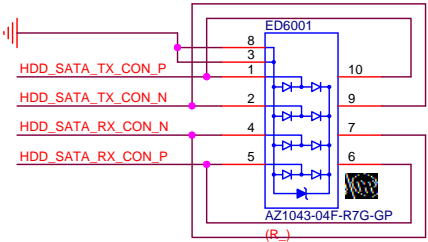
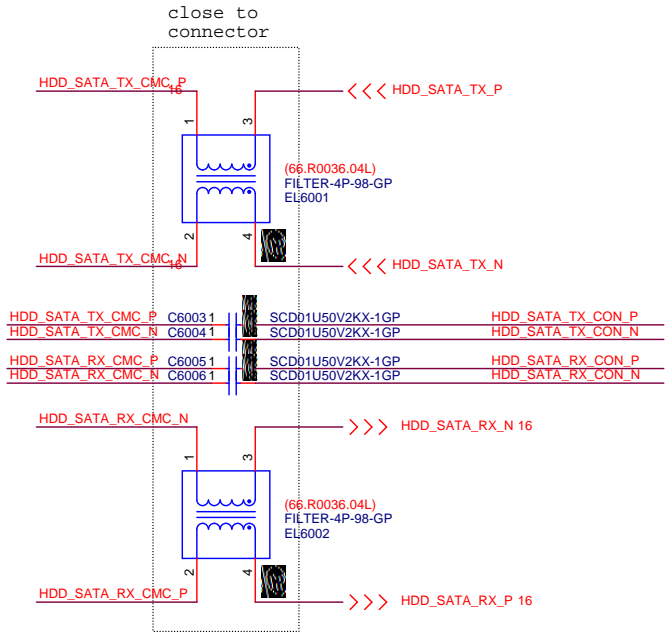
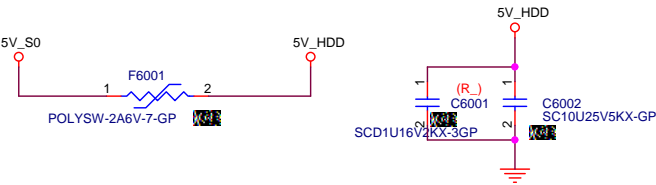
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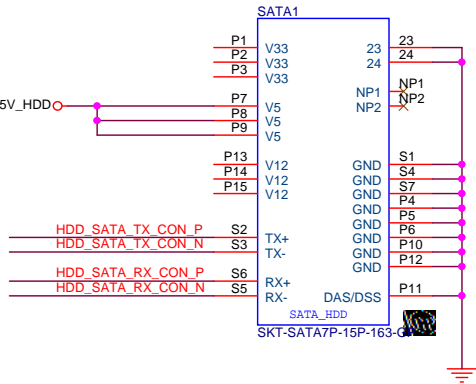
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Display (RSVD) Backlight PW		
Size A	Document Number Eiffel-2 ICL U	Rev SA
Date: Friday, December 27, 2019	Sheet 59	of 106

SATA HDD Connector

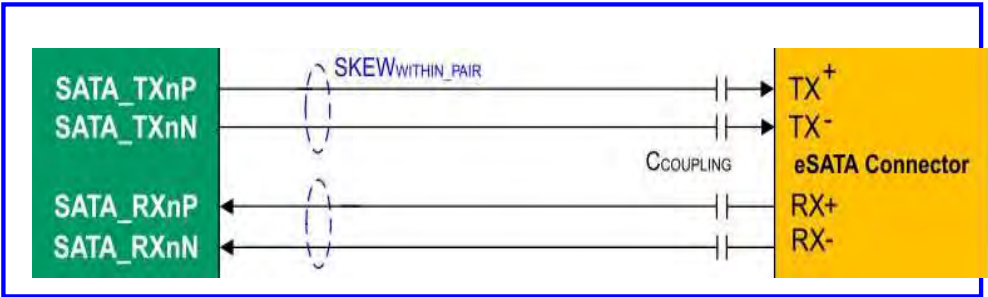
Layout: Put them together



HDD CONN



2017/08/14 Damon Wei Modify
SATA1 change F7 from (022.10019.0061) to (022.10019.0021)



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<div>緯創資通</div>		<div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div> <div>INT IO (RSVD) WWAN</div>			
<div>Size</div> <div>A</div>	<div>Document Number</div> <div>Eiffel-2 ICL U</div>		<div>Rev</div> <div>SA</div>
<div>Date:</div> <div>Friday, December 27, 2019</div>	<div>Sheet</div> <div>62</div>	<div>of</div>	<div>106</div>

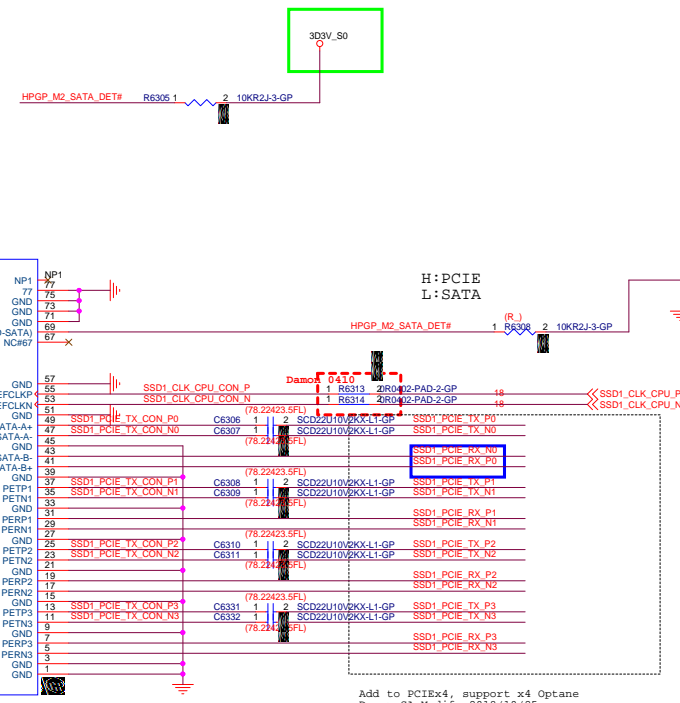
M.2 SSD

SSD1_PCIE_TX_P0
SSD1_PCIE_TX_N0
SSD1_PCIE_RX_N0
SSD1_PCIE_RX_P0
SSD1_PCIE_TX_P1
SSD1_PCIE_TX_N1
SSD1_PCIE_RX_P1
SSD1_PCIE_RX_N1
SSD1_PCIE_TX_P2
SSD1_PCIE_TX_N2
SSD1_PCIE_RX_P2
SSD1_PCIE_RX_N2
SSD1_PCIE_TX_P3
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SSD1_PCIE_RX_N3
HPGP_M2_SATA_DET#
GPP_H0

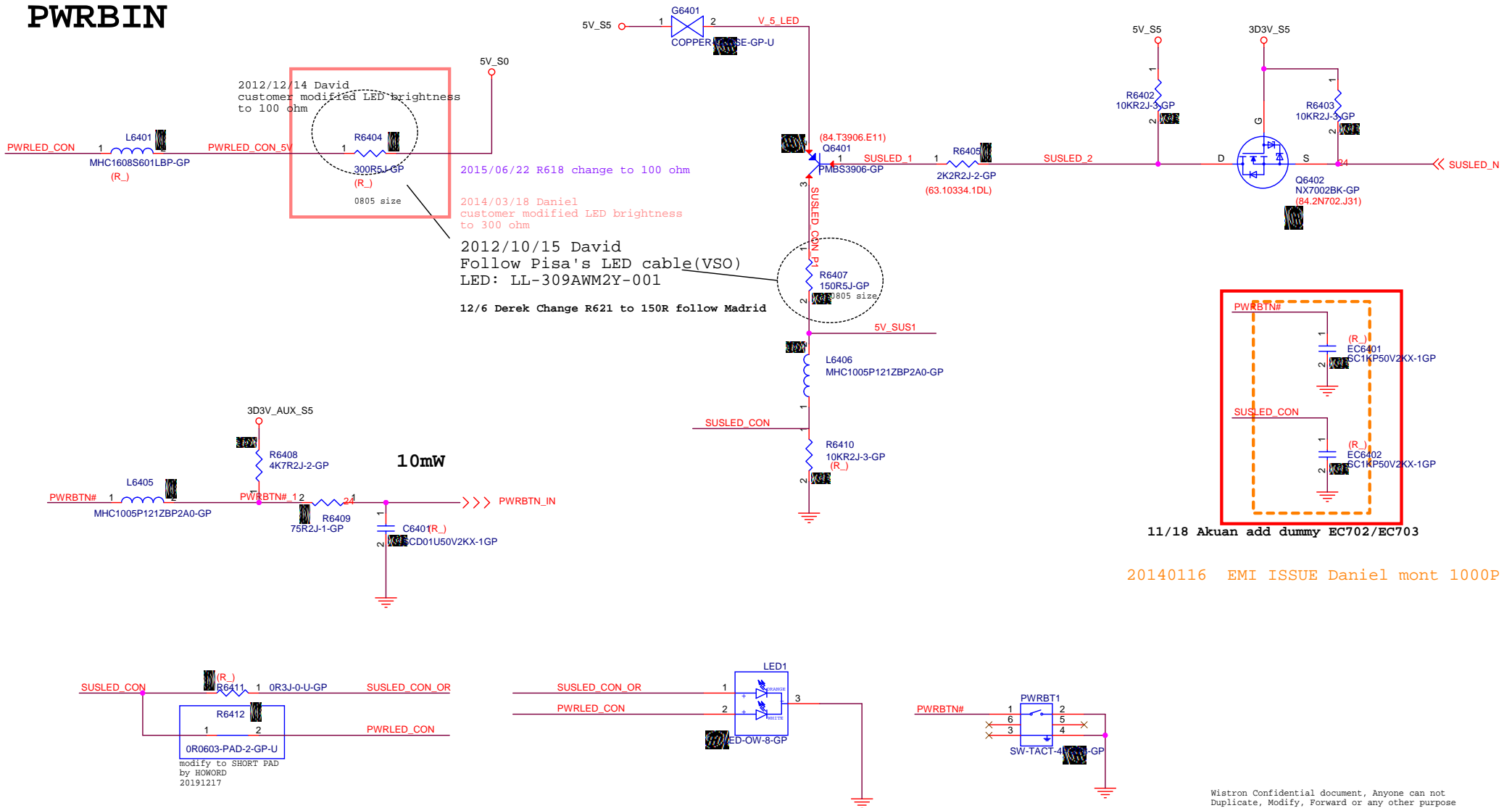
HPGP_M2_SATA_DET#	Module Type
0	SSD-SATA
1	SSD-PCIE

M.2 Key M Type

Change NGFFM1 CONN to 062.10003.0701, follow CE advice
Damon Wei SA Modify 2018/12/07



PWRBIN



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<Variant Name>

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Title	LED / Button / Power Button
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Size B	Document Number Eiffel-2_ICL_U	Rev SA
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Date: Friday, December 27, 2019 Sheet 64 of 106

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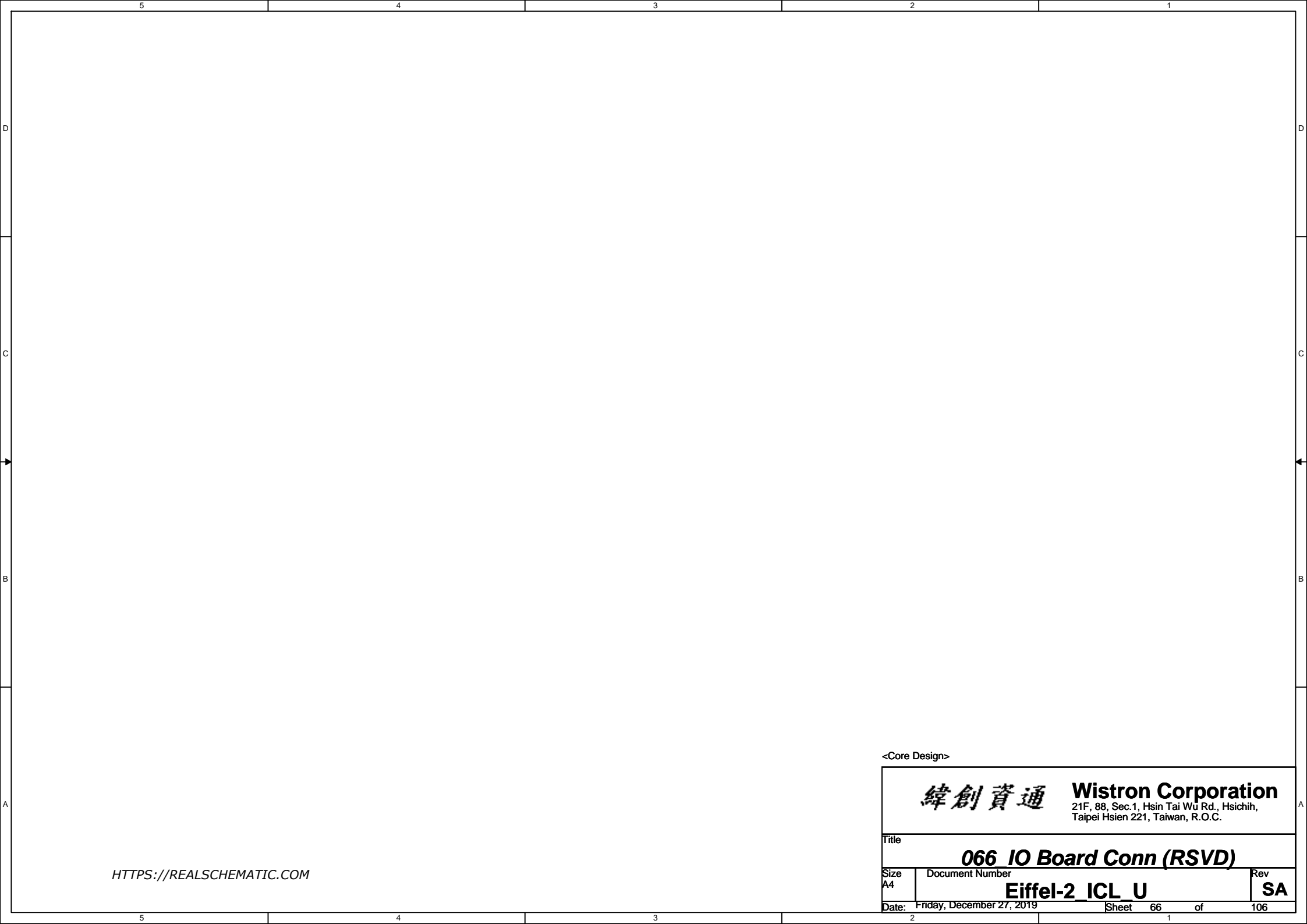
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Title		
INT IQ (Key BoardTouch Pad)		
Size	Document Number	Rev
Custom	Eiffel-2 ICL U	SA
Date: Friday, December 27, 2019	Sheet 65 of	106



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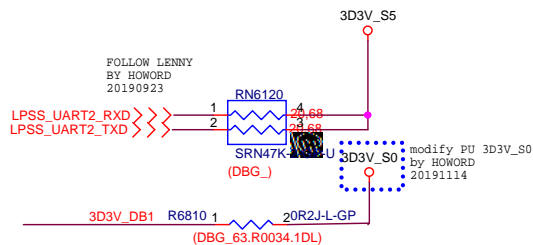
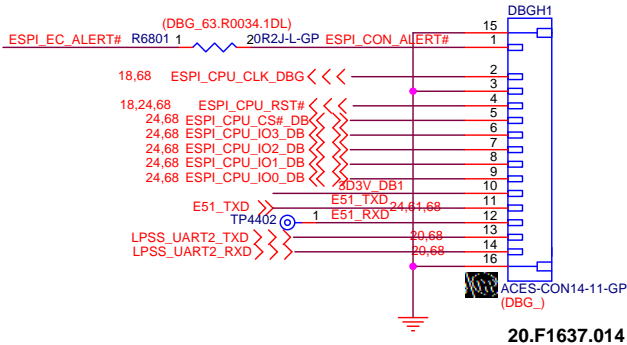
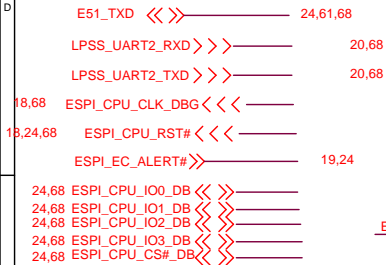
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Title <div>066 IO Board Conn (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Eiffel-2_ICL_U</div>	Rev <div>SA</div>
Date: Friday, December 27, 2019		Sheet 66 of 106

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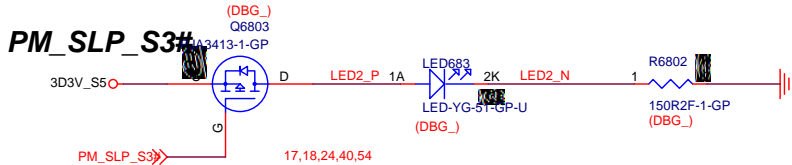
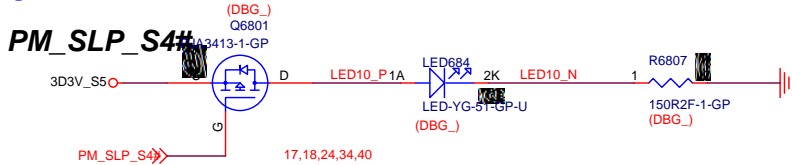
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title067_Sensor (Hall Sensor/Vol BOT		
SizeA4	Document NumberEiffel-2_ICL_U	RevSA
Date: Friday, December 27, 2019	Sheet 67	of 106

LPC DEBUG PORT

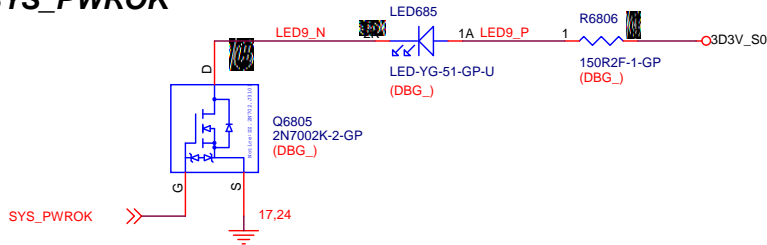


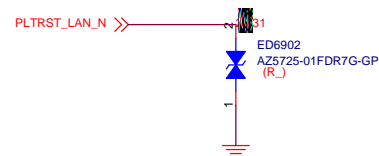
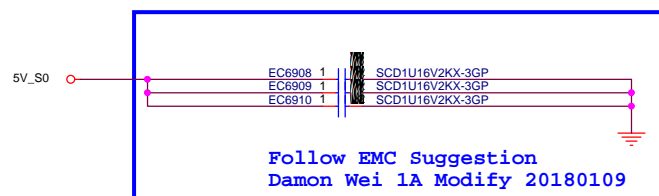
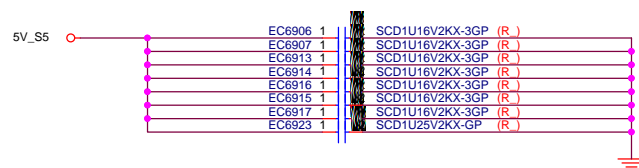
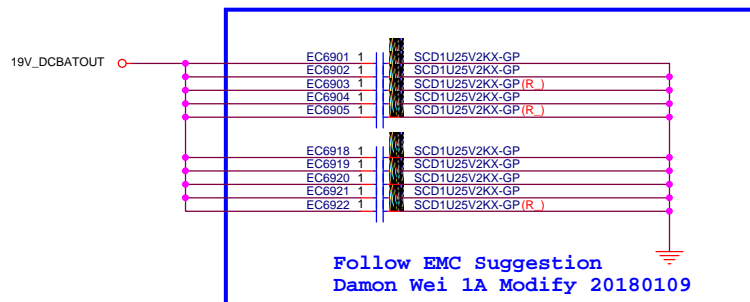
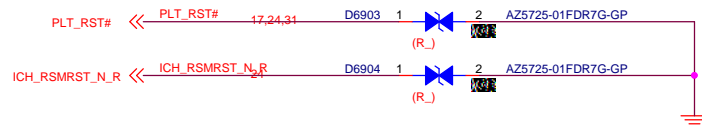
Add Debug Led,follow Mocha.
Damon SA Modify 11/17

Debug LED



SYS_PWROK





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Title 069_Sensor (RSVD) (GYROSCOPE)		
Size A3	Document Number	Rev SA
Date: Friday, December 27, 2019	Sheet 69 of 106	



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緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

070 Sensor (RSVD)

Size

Document Number

Rev

A3Eiffel-2 ICL USA

Date: Friday, December 27, 2019

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Title		
072 EXT IO (Type-C CC-logic)		
Size	Document Number	Rev
A2	Eiffel-2 ICL U	SA
Date	Friday, October 27, 2018	Sheet 72 of 108

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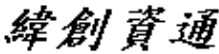
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083 GPU (RSVD) (VRAM 5.6 3/4)

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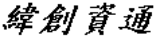
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084 GPU (RSVD) (VRAM 7.8 4/4)

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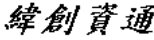
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086 GPU (VGA POWER AOZ2260)

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088_(RSVD)

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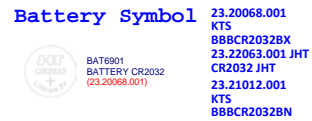
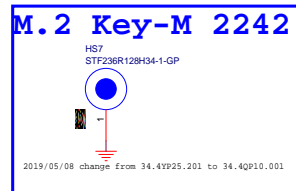
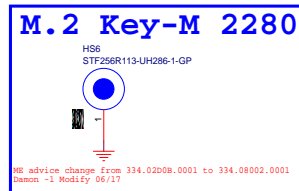
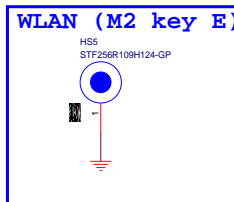
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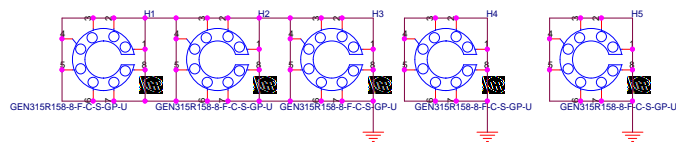
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Date: Friday, December 27, 2019

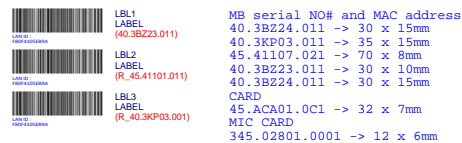
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Scre Hole (PCB New type MOUNTING HOLES)



LABEL



Heatsink Symbol



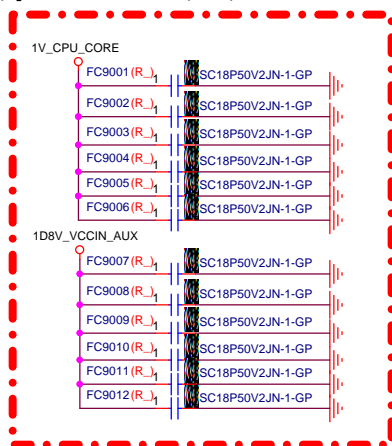
PCB Symbol



Part Number	Manufacture (Gerber Out)
348.09008.008A	CEE (Yes)
348.09009.008A	HANSTAS (Yes)
348.09010.008A	GLOBALBRAN (Yes)

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(SI add) place close to CPU (<5mm)



place close to DDR

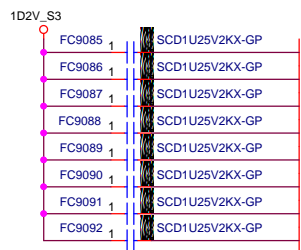


Table 9-1. VCCIN and VCCIN_AUX Decoupling Capacitors

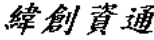
	Cap. Placement	Capacitance
VCCIN	<= 5mm from SoC	6x15 pF (0201) or 6x12 pF (0402)
VCCIN_AUX HTTPS://REALSCHEMATIC.COM	<= 5mm from SoC	6x15 pF (0201) or 6x12 pF (0402)

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091_INT IO (TPM)

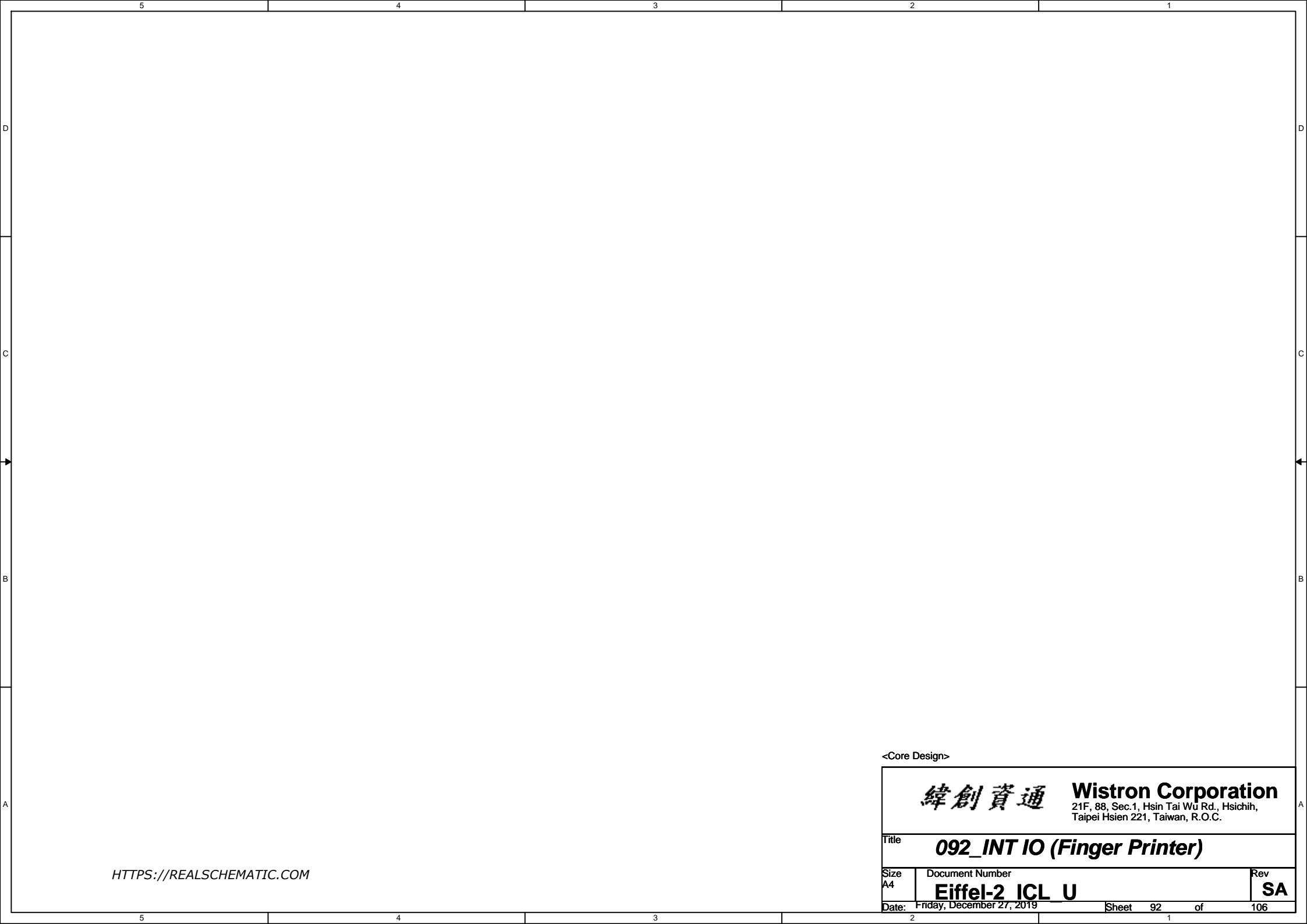
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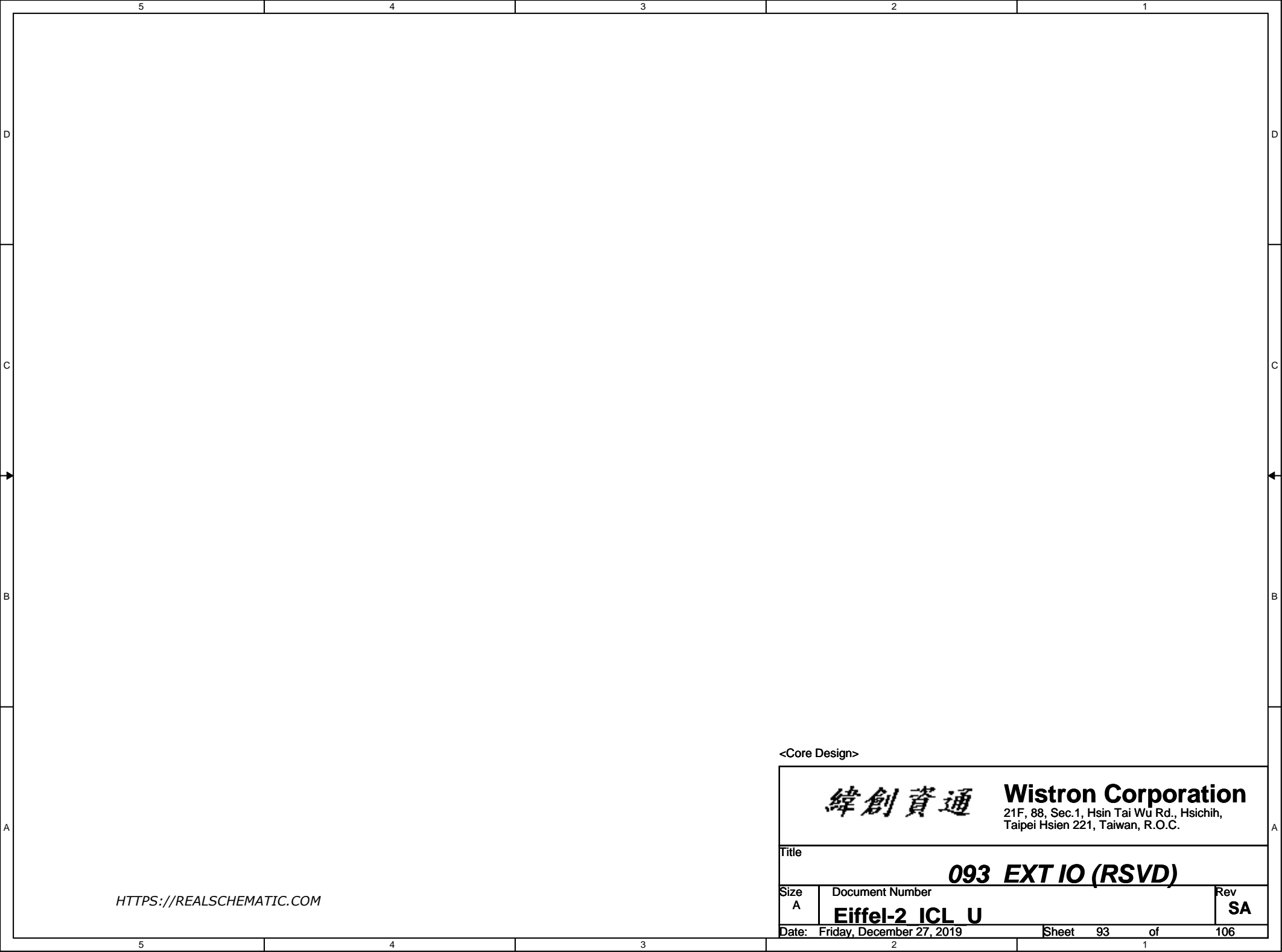
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Title <div>092_INT IO (Finger Printer)</div>		
Size <div>A4</div>	Document Number <div>Eiffel-2 ICL U</div>	Rev <div>SA</div>
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095 EXT IO (RSVD)			
Size A2	Document Number		Rev
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Title			
096 Commercial (RSVD)			
Size	Project Name		Rev
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A

B

C

D

E

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1

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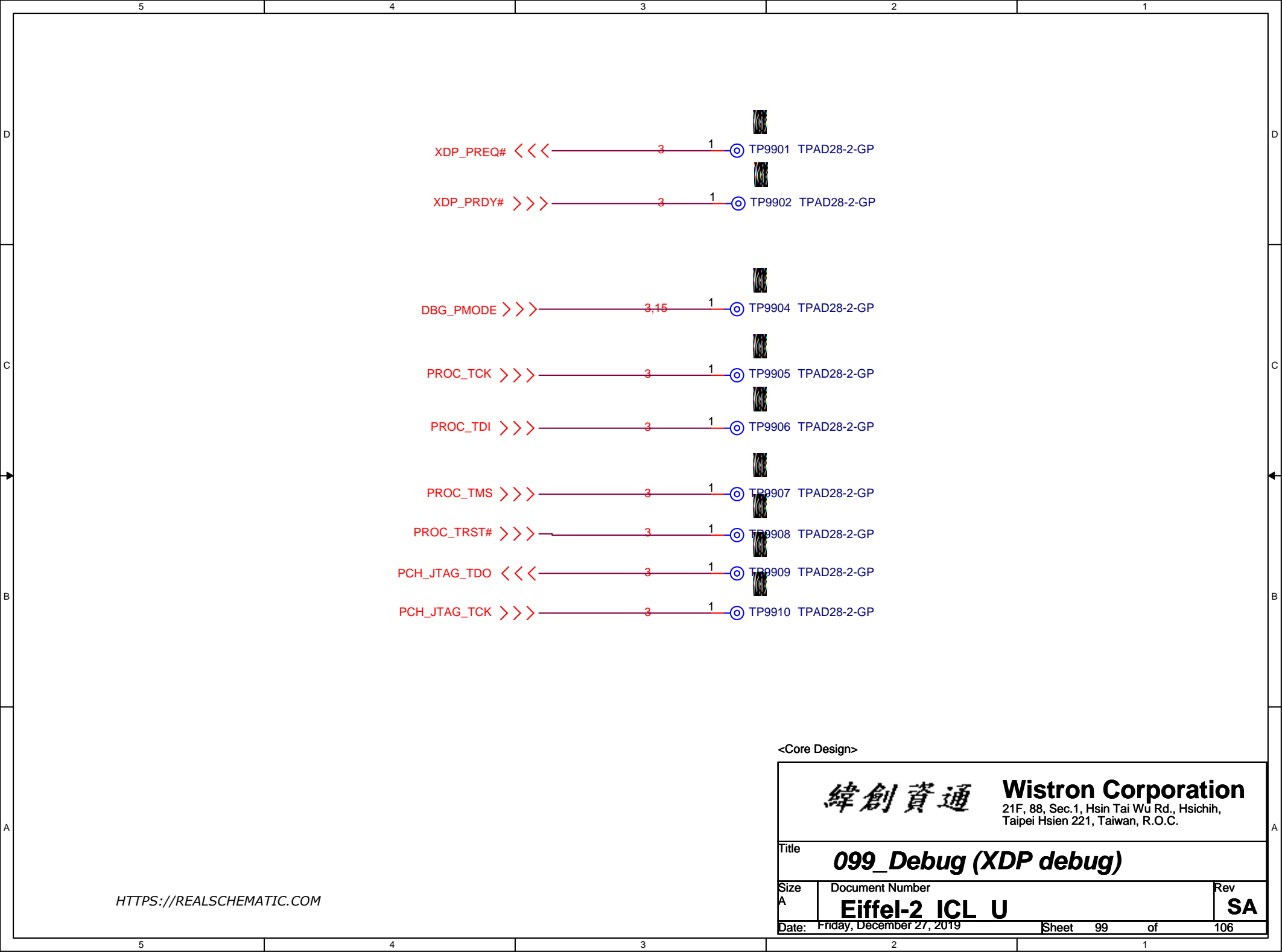
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Title			
097 Commercial (RSVD)			
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Title <div>099_Debug (XDP debug)</div>		
Size <div>A</div>	Document Number <div>Eiffel-2 ICL U</div>	Rev <div>SA</div>
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101_Change History

Size

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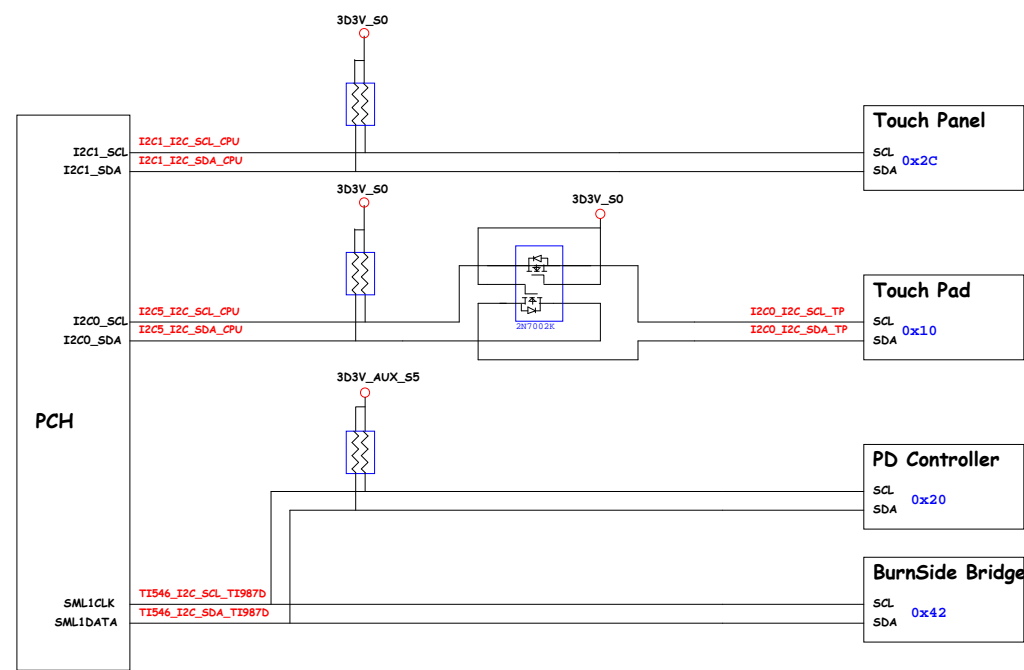
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Table 11-23. System with M3 State Supported

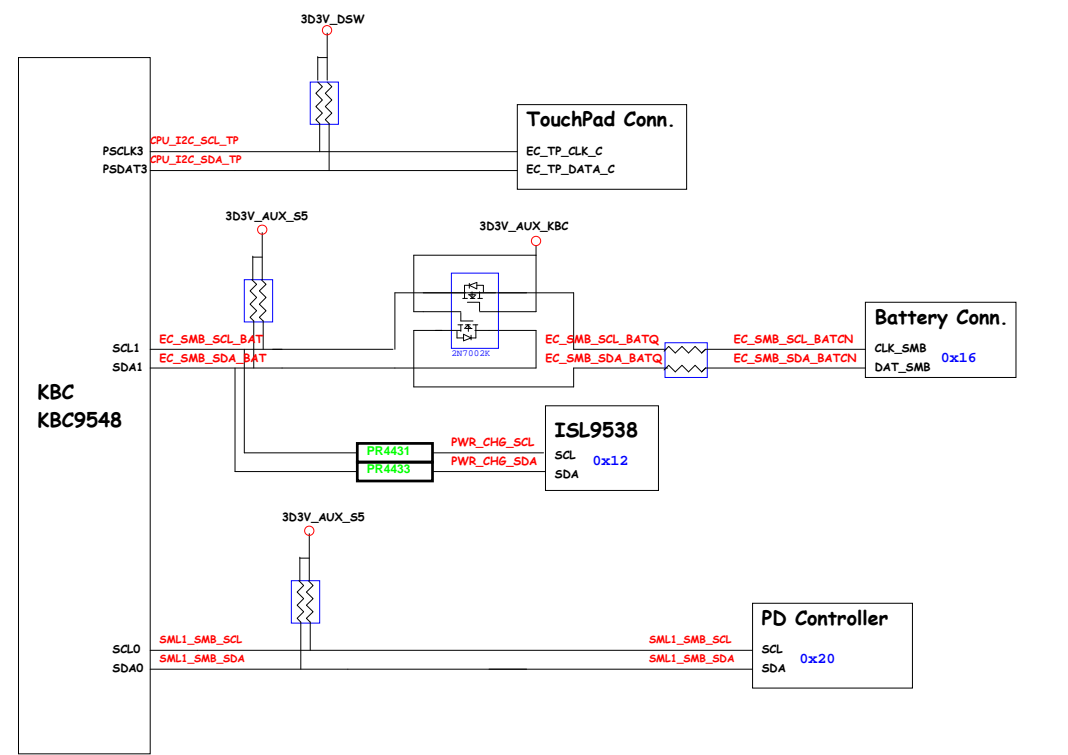
Notes:

- 1. The state of the system without ETC can be powered on also as considered in G3.
- 2. VCC2G, VCC3G, OC, TCSS, ADRG can be turned off when the processor is in C32
- 3. VCC1G, VCC2G, VCC3G, OC, TCSS, ADRG, VCC4G, VCC5G, VCC6G, VCC7G, VCC8G, VCC9G, VCC10G, VCC11G, VCC12G, VCC13G, VCC14G, VCC15G, VCC16G, VCC17G, VCC18G, VCC19G, VCC20G, VCC21G, VCC22G, VCC23G, VCC24G, VCC25G, VCC26G, VCC27G, VCC28G, VCC29G, VCC30G, VCC31G, VCC32G, VCC33G, VCC34G, VCC35G, VCC36G, VCC37G, VCC38G, VCC39G, VCC40G, VCC41G, VCC42G, VCC43G, VCC44G, VCC45G, VCC46G, VCC47G, VCC48G, VCC49G, VCC50G, VCC51G, VCC52G, VCC53G, VCC54G, VCC55G, VCC56G, VCC57G, VCC58G, VCC59G, VCC60G, VCC61G, VCC62G, VCC63G, VCC64G, VCC65G, VCC66G, VCC67G, VCC68G, VCC69G, VCC70G, VCC71G, VCC72G, VCC73G, VCC74G, VCC75G, VCC76G, VCC77G, VCC78G, VCC79G, VCC80G, VCC81G, VCC82G, VCC83G, VCC84G, VCC85G, VCC86G, VCC87G, VCC88G, VCC89G, VCC90G, VCC91G, VCC92G, VCC93G, VCC94G, VCC95G, VCC96G, VCC97G, VCC98G, VCC99G, VCC100G, VCC101G, VCC102G, VCC103G, VCC104G, VCC105G, VCC106G, VCC107G, VCC108G, VCC109G, VCC110G, VCC111G, VCC112G, VCC113G, VCC114G, VCC115G, VCC116G, VCC117G, VCC118G, VCC119G, VCC120G, VCC121G, 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PCH SMBus Block Diagram



KBC SMBus Block Diagram



Audio Block Diagram

